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Zdeblick

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(54) **METHODS AND APPARATUS FOR LEADS FOR IMPLANTABLE DEVICES**

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(52) **U.S. Cl.** **607/115**; 607/9; 607/36; 607/37

(58) **Field of Classification Search** 607/9, 115, 607/36–37

See application file for complete search history.

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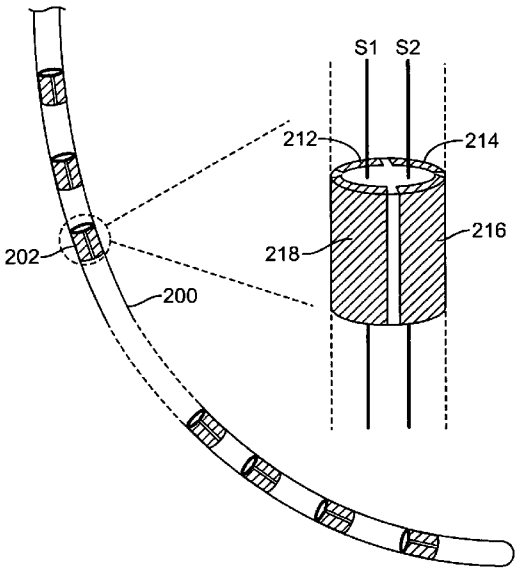
(57) **ABSTRACT**

A charge pump is provided in the same integrated circuit chip as a control means which permits selectively connecting any of one or more electrodes with conductors along a lead. The charge pump derives about two volts from a one-volt supply, and becomes stable within a few tens of microseconds. The charge pump may be composed of three doublers—the first generating timing signals for the second and third doublers, with the second and third doublers working out of phase with each other.

10 Claims, 6 Drawing Sheets



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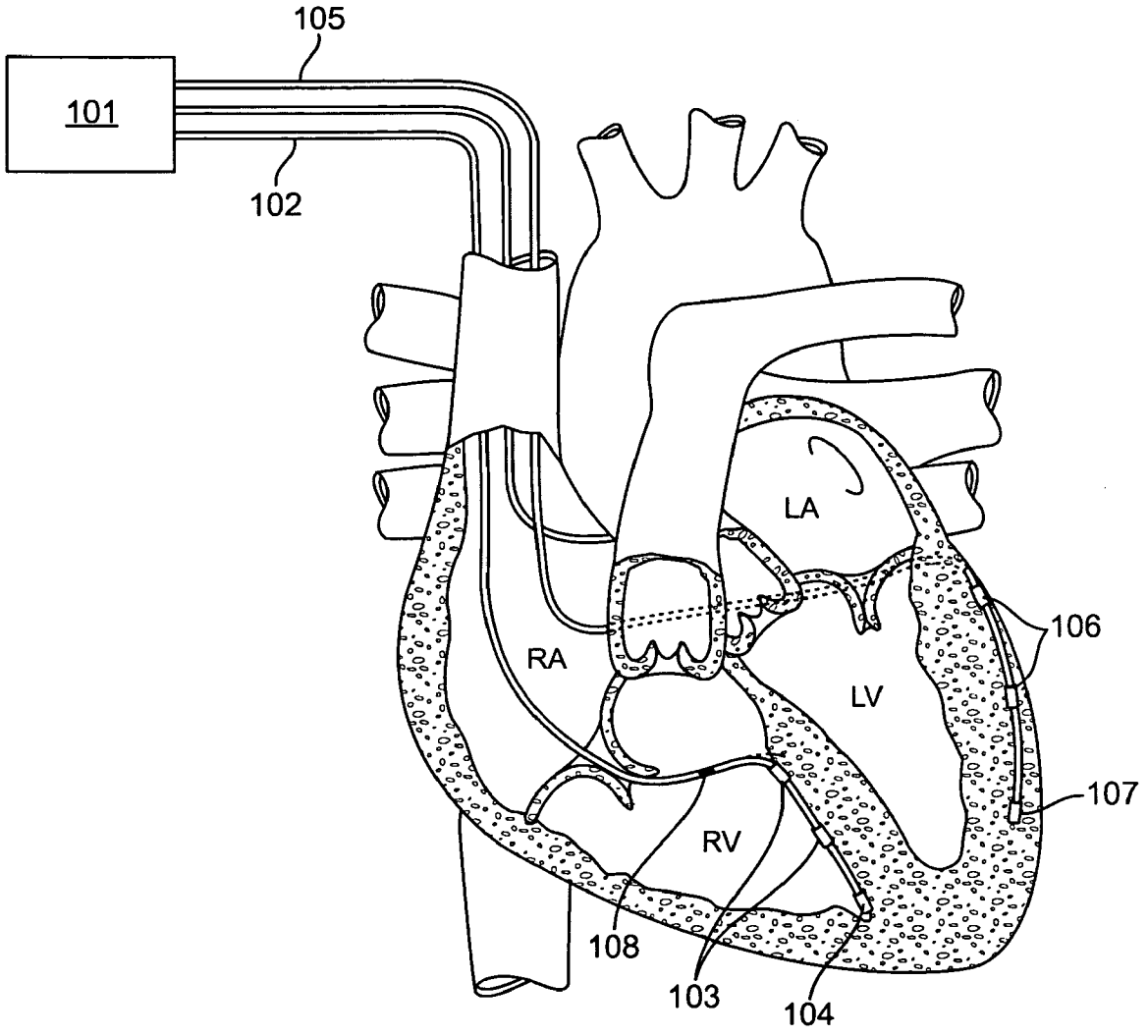


FIG. 1

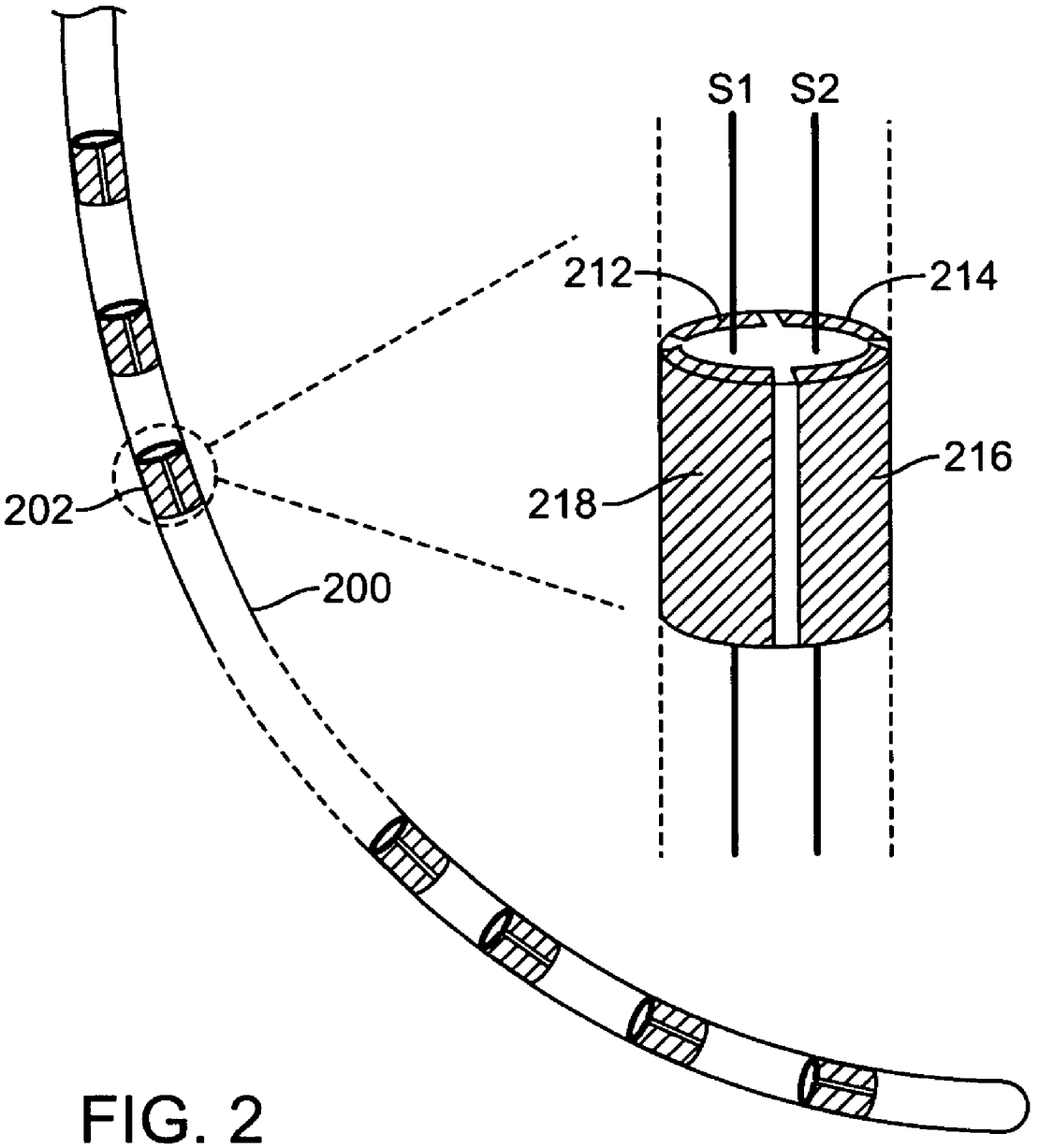


FIG. 2

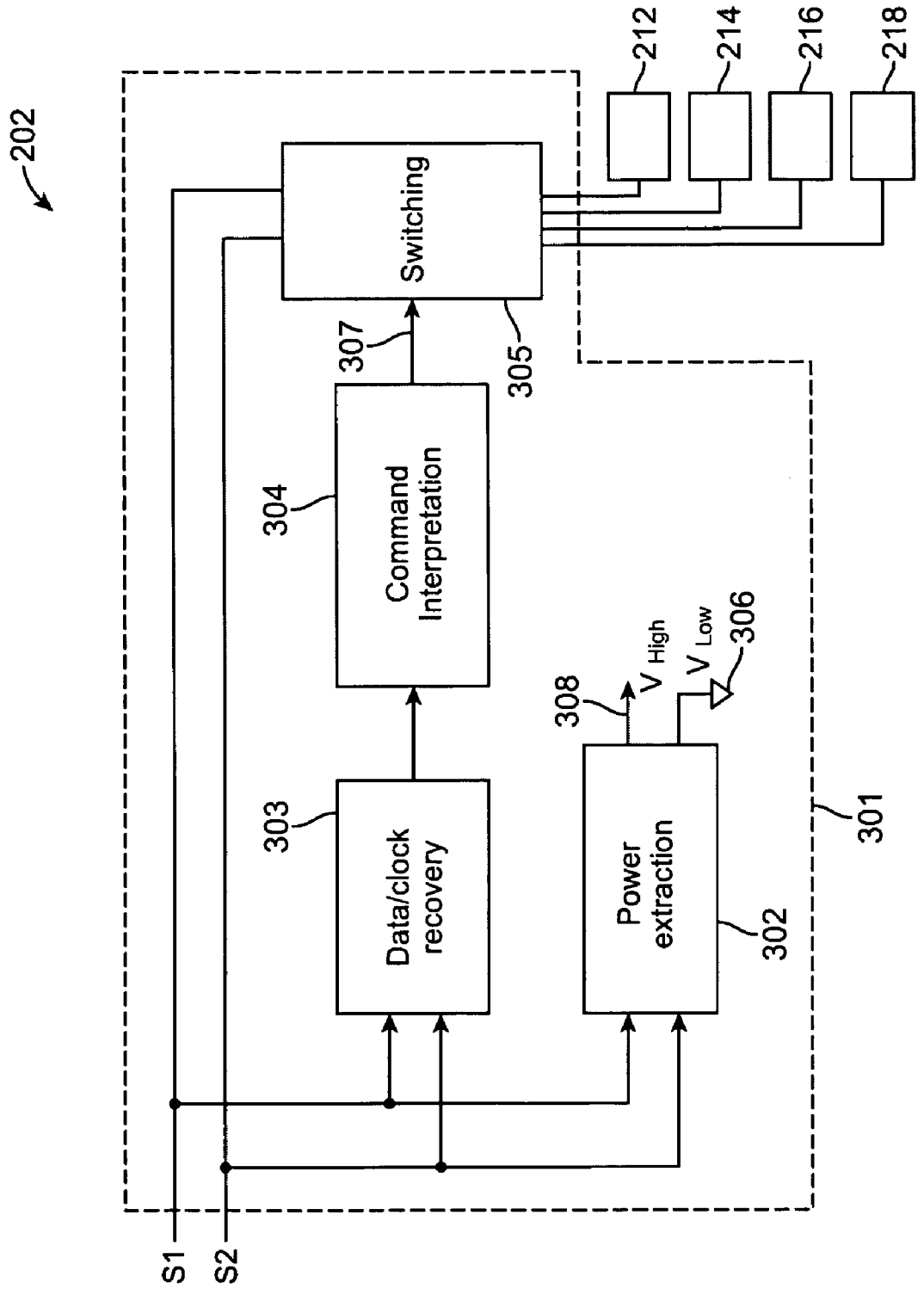

202
212
214
216
218
Switching
305
307
304
Command Interpretation
303
Data/clock recovery
308
V_{High}
V_{Low}
306
Power extraction
302
301
S1
S2

FIG. 3

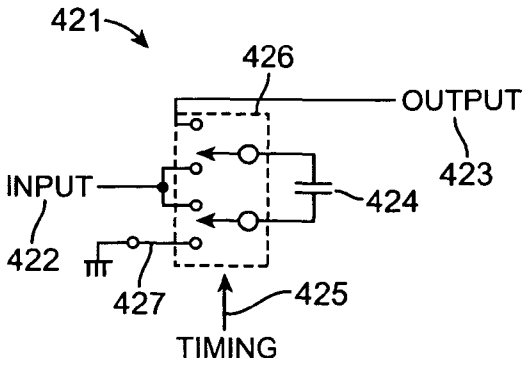


FIG. 4

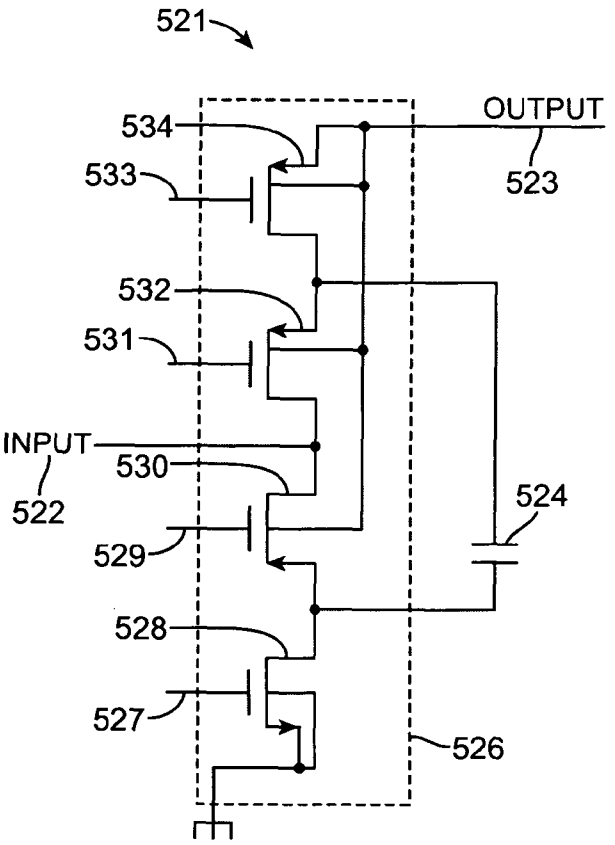


FIG. 5

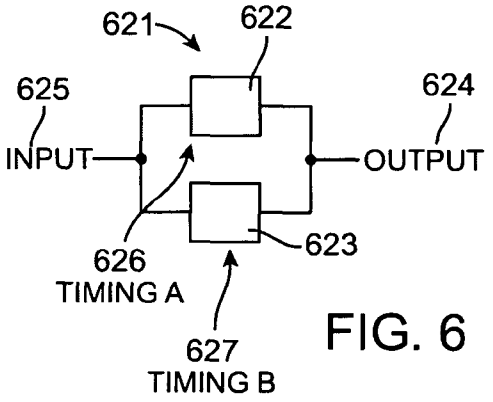


FIG. 6

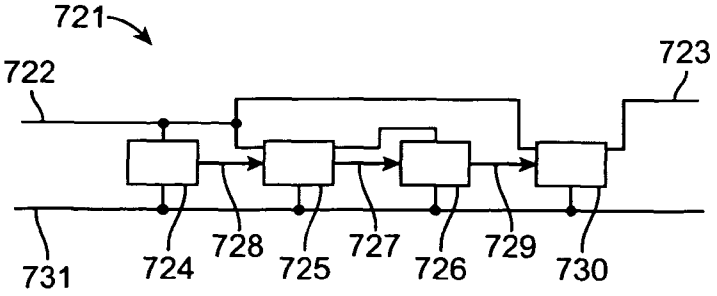


FIG. 7

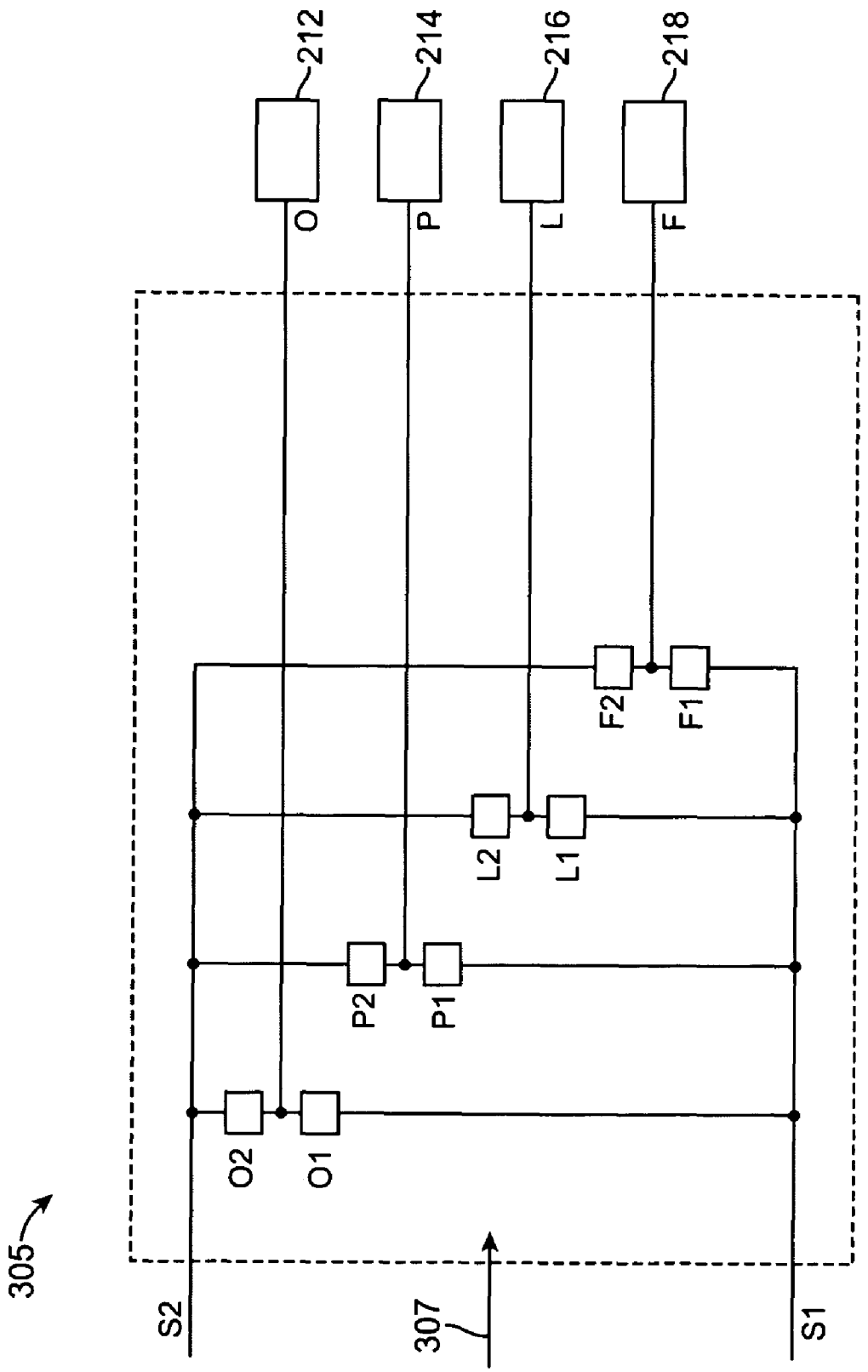
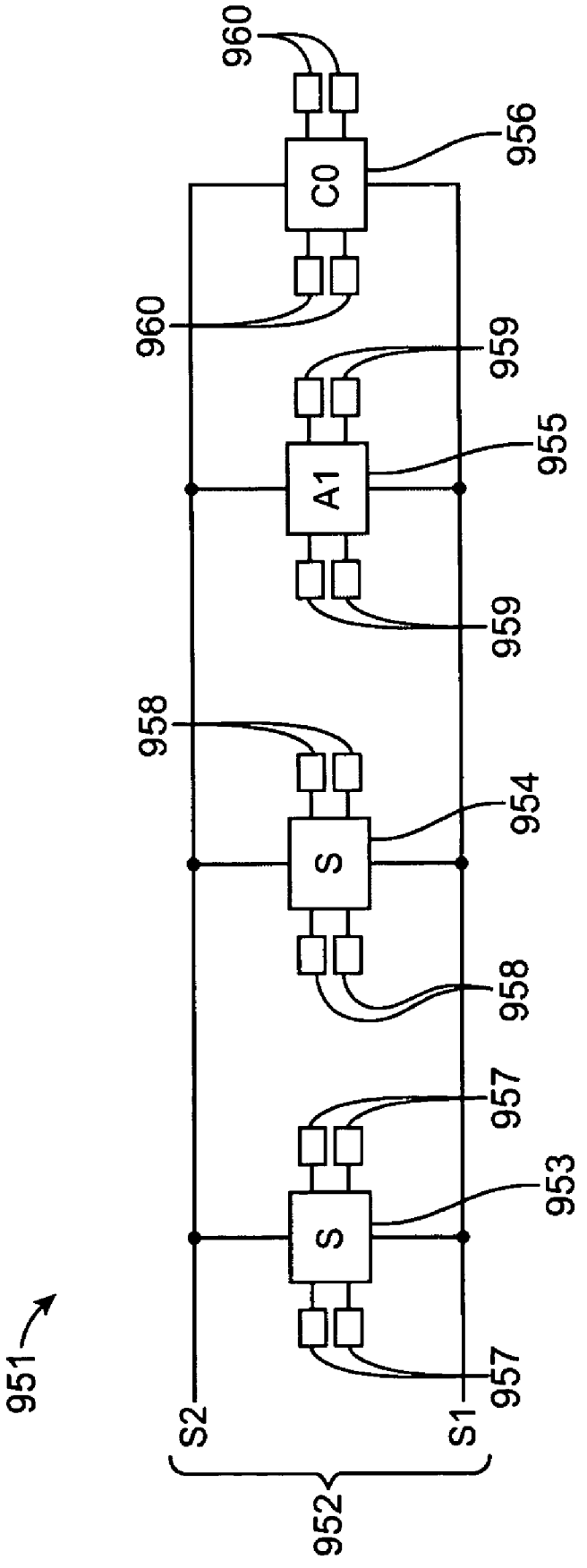


FIG. 8


960
956
C0
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A1
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958
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S
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S
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951
S2
S1
952

FIG. 9

METHODS AND APPARATUS FOR LEADS FOR IMPLANTABLE DEVICES

BACKGROUND

It is not easy to make leads for implantable devices that work well when connected with legacy implantable devices, and yet that also offer sophisticated functions such as addressability when used with modern-day implantable devices, and that further offer the flexibility to work with implantable devices not yet devised.

A typical example of an implantable device is a cardiac pacemaker. Other implantable devices include defibrillators, drug delivery systems, neurological stimulators, and bone growth stimulators.

One of the many challenges facing the designer of a lead is the problem that the designer is not permitted to make very many assumptions about the power provided to the lead by the external equipment such as a pacemaker. The power may be of very limited voltage, perhaps as little as one volt. Yet the main circuitry of the chip in each satellite of the lead is likely to require about two volts to carry out its tasks.

SUMMARY OF THE INVENTION

A voltage doubler or charge pump is provided in the same integrated circuit chip as a control means which permits selectively connecting any of one or more electrodes with conductors along a lead. The voltage doubler derives about two volts from a one-volt supply, and becomes stable within a few tens of microseconds. The voltage doubler may be composed of three doublers—the first generating timing signals for the second and third doublers, with the second and third doublers working out of phase with each other.

DESCRIPTION OF THE DRAWING

The invention will be described with respect to a drawing in several figures, of which:

FIG. **1** shows an implantable device **101** and leads including lead **102** implanted in a human heart;

FIG. **2** shows a lead **200** of a type employed in FIG. **1**, having satellites **202**;

FIG. **3** is a functional block diagram of a satellite **202** as shown in FIG. **2**;

FIG. **4** shows a classic flying-capacitor voltage doubler as is well known in the art;

FIG. **5** shows in schematic detail a voltage doubler as employed in the apparatus according to the invention;

FIG. **6** shows two voltage doublers excited out of phase with each other, so as to provide better power generation;

FIG. **7** shows cascaded voltage doublers according to the invention;

FIG. **8** shows a switching circuitry as might be used in the integrated circuit of the satellite of FIG. **3**; and

FIG. **9** shows four chips of three different types disposed along a lead.

Where possible, like elements among the figures have been designated with like reference numerals, for convenience of notation.

DETAILED DESCRIPTION

An implantable pulse generator according to an embodiment of the invention is depicted in FIG. **1**. FIG. **1** illustrates locations of a number of pacing satellites incorporated in multi-electrode pacing leads, in accordance with an embodiment of the present invention. A pacing and signal detection system **101** provides extra-cardiac communication and control elements for the overall system. In some embodiments, pacing and signal detection system **101** may be, for example, a pacing can of a pacemaker residing in an external or extra-corporeal location.

Right ventricular lead **102** emerges from pacing and signal detection system **101** and travels from a subcutaneous location from pacing and signal detection system **101** into the patient's body (e.g., preferably, a subclavian venous access), and through the superior vena cava into the right atrium. From the right atrium, right ventricle lead **102** is threaded through the tricuspid valve to a location along the walls of the right ventricle. The distal portion of right ventricular lead **102** is preferably located along the intra-ventricular septum, terminating with a fixation in the right ventricular apex. Right ventricular lead **102** includes satellites positioned at locations **103** and **104**.

The number of satellites in ventricular lead **102** is not limited, and may be more or less than the number of satellites shown in FIG. **1**.

Similarly, left ventricular lead **105** emerges from the pacing and signal detection system **101**, following substantially the same route as right ventricular lead **102** (e.g., through the subclavian venous access and the superior vena cava into the right atrium). In the right atrium, left ventricular lead **105** is threaded through the coronary sinus around the posterior wall of the heart in a cardiac vein draining into the coronary sinus. Left ventricular lead **105** is provided laterally along the walls of the left ventricle, which is likely to be an advantageous position for bi-ventricular pacing. FIG. **1** shows satellites positioned at locations **106** and **107** along left ventricular lead **105**. Right ventricular lead **102** may optionally be provided with pressure sensor **108** in the right ventricle. A signal multiplexing arrangement allows a lead to include such active devices (e.g., pressure sensor **108**) for pacing and signal collection purposes (e.g., right ventricular lead **102**). Pacing and signal detection system **101** communicates with each of the satellites at locations **103**, **104**, **106** and **107**. The electrodes controlled by the satellites may also be used to detect cardiac depolarization signals. Additionally, other types of sensors, such as an accelerometer, strain gauge, angle gauge, temperature sensor, can be included in any of the leads.

In the above system, the device components can be connected by a multiplex system (e.g., as described U.S. Pat. No. 7,214,189, U.S. patent application Ser. No. 10/734,490 published as 20040193021 (pending), U.S. patent application Ser. No. 11/793,904 published as 20080255647 (pending) and U.S. patent application Ser. No. 11/794,016 published as 20080312726 (pending); the disclosures of which are herein incorporated by reference), to the proximal end of electrode lead **105** The proximal end of electrode lead **105** connects to a pacemaker **101**, e.g., via an IS-1 connector.

During certain embodiments of use, the electrode lead **105** is placed in the heart using standard cardiac lead placement devices which include introducers, guide catheters, guidewires, and/or stylets. Briefly, an introducer is placed into the clavicle vein. A guide catheter is placed through the introducer and used to locate the coronary sinus in the right atrium. A guidewire is then used to locate a left ventricle cardiac vein. The electrode lead **105** is slid over the guidewire into the left ventricle cardiac vein and tested until an optimal location for CRT is found. Once implanted a multi-electrode lead **105** still allows for continuous readjustments of the optimal electrode location. The electrode lead **102** is placed in the right ventricle of the heart. In this view, the electrode lead **102** is provided with one or multiple electrodes **103**, **104**.

Electrode lead **102** is placed in the heart in a procedure similar to the typical placement procedures for cardiac right ventricle leads. Electrode lead **102** is placed in the heart using the standard cardiac lead devices which include introducers, guide catheters, guidewires, and/or stylets. Electrode lead **102** is inserted into the clavicle vein, through the superior vena cava, through the right atrium and down into the right ventricle. Electrode lead **102** is positioned under fluoroscopy into the location the clinician has determined is clinically optimal and logistically practical for fixating the electrode lead **102**.

Summarizing aspects of the above description, in using the implantable pulse generators of the invention, such methods include implanting an implantable pulse generator e.g., as described above, into a subject; and the implanted pulse generator, e.g., to pace the heart of the subject, to perform cardiac resynchronization therapy in the subject, etc. The description of the present invention is provided herein in certain instances with reference to a subject or patient. As used herein, the terms "subject" and "patient" refer to a living entity such as an animal. In certain embodiments, the animals are "mammals" or "mammalian," where these terms are used broadly to describe organisms which are within the class mammalia, including the orders carnivore (e.g., dogs and cats), rodentia (e.g., mice, guinea pigs, and rats), lagomorpha (e.g. rabbits) and primates (e.g., humans, chimpanzees, and monkeys). In certain embodiments, the subjects, e.g., patients, are humans.

During operation, use of the implantable pulse generator may include activating at least one of the electrodes of the pulse generator to deliver electrical energy to the subject, where the activation may be selective, such as where the method includes first determining which of the electrodes of the pulse generator to activate and then activating the electrode. Methods of using an IPG, e.g., for pacing and CRT, are disclosed in U.S. Pat. No. 7,214,189 entitled "Methods and apparatus for tissue activation and monitoring"; US publication number US 2008-0255647 entitled "Implantable addressable segmented electrodes" (pending); PCT publication number WO 2006/069323 entitled "Implantable hermetically sealed structures" (pending); international patent publication number WO 2007/075974 entitled "Implantable integrated circuit" (pending); and US patent publication US 2008-0077186 entitled "High phrenic, low capture threshold pacing devices and methods" (pending); the disclosures of the various methods of operation of these applications being herein incorporated by reference and applicable for use with the present devices.

FIG. **2** is an external view of a number of exemplary pacing satellites, in accordance with a multiplex lead embodiment of the present invention. According to one embodiment, a pacing lead **200** (e.g., right ventricular lead **102** or left ventricular lead **105** of FIG. **1**) accommodates two bus wires S**1** and S**2**, which are coupled to a number (e.g., eight) of satellites, such as satellite **202**. S**2**, in an exemplary embodiment, is an anode conductor, and **51** is a cathode conductor. FIG. **2** also shows satellite **202** with an enlarged view. Satellite **202** includes electrodes **212**, **214**, **216**, and **218**, located in the four quadrants of the cylindrical outer walls of satellite **202** and supported by a support structure of the invention. Each satellite also contains a control chip inside the structure which communicates with a pacing and signal-detection system to receive configuration signals that determine which of the four electrodes is to be coupled to bus wires S**1** or S**2**.

The configuration signals, the subsequent pacing pulse signals, and the analog signals collected by the electrodes can all be communicated through bus wires S**1** and S**2**, in either direction. Although shown in a symmetrical arrangement, electrodes **212**, **214**, **216** and **218** may be offset along lead **200** to minimize capacitive coupling among these electrodes. The quadrant arrangement of electrodes allows administering pacing current via electrodes oriented at a preferred direction, for example, away from nerves, or facing an electrode configured to sink the pacing current. Such precise pacing allows low-power pacing and minimal tissue damage caused by the pacing signal.

The leads may further include a variety of different effector elements, which elements may employ the satellites or structures distinct from the satellites. The effectors may be intended for collecting data, such as but not limited to pressure data, volume data, dimension data, temperature data, oxygen or carbon dioxide concentration data, hematocrit data, electrical conductivity data, electrical potential data, pH data, chemical data, blood flow rate data, thermal conductivity data, optical property data, cross-sectional area data, viscosity data, radiation data and the like. As such, the effectors may be sensors, e.g., temperature sensors, accelerometers, ultrasound transmitters or receivers, voltage sensors, potential sensors, current sensors, etc. Alternatively, the effectors may be intended for actuation or intervention, such as providing an electrical current or voltage, setting an electrical potential, heating a substance or area, inducing a pressure change, releasing or capturing a material or substance, emitting light, emitting sonic or ultrasound energy, emitting radiation and the like.

Effectors of interest include, but are not limited to, those effectors described in the following applications by at least some of the inventors of the present application: U.S. Patent publication number US 20040193021 entitled "Method And System For Monitoring And Treating Hemodynamic Parameters" (pending); U.S. Patent publication number US 20060058588 entitled "Methods And Apparatus For Tissue Activation And Monitoring" (patented with issue no. of 7,214,189); International patent publication number WO 2006/069323 (pending); U.S. Patent publication no. US 2006-0161211 entitled "Implantable Accelerometer-Based Cardiac Wall Position Detector" (pending); U.S. Pat. No. 7,200,439 entitled "Method and Apparatus for Enhancing Cardiac Pacing"; U.S. Pat. No. 7,204,798 entitled "Methods and Systems for Measuring Cardiac Parameters"; U.S. Pat. No. 7,267,649 entitled "Method and System for Remote Hemodynamic Monitoring"; U.S. patent publication no. US 2006-0217793 entitled "Fiberoptic Tissue Motion Sensor" (patented with issue no. of 7,837,634); U.S. Pat. No. 7,028,550 entitled "Implantable Pressure Sensors"; U.S. Patent publication No. US 2006-0116581 entitled "Implantable Doppler Tomography System" (patented with issue no. of 7,925,329); and US patent publication US 2008-0255629 (pending) entitled "Cardiac Motion Characterization by Strain Measurement". These applications are incorporated in their entirety by reference herein.

A typical satellite **202** (shown in FIG. **2**) is shown in more detail in FIG. **3**. Conductors S**1**, S**2** are shown, connecting with an IC (integrated circuit) **301**, which is a six-terminal device. The other four terminals are connection points to electrodes **212**, **214**, **216**, and **218** (also visible in FIG. **2**).

IC **301** includes a power extraction block **302**, a data and clock recovery block **303**, a command interpretation block **304**, and a switching block **305**.

The power extraction block **302** obtains DC power from the conductors S**1**, S**2**, and makes the power available for use in other parts of the IC **301**, for example as power line Vhigh and ground.

The data and clock recovery block **303** detects a clock signal from conductors S**1**, S**2**, and uses the clock signal to

time the sampling of the conductors S1, S2 to detect data on the conductors S1, S2. A command interpretation block **304** receives data from the block **303** and picks out commands from the data.

The switching block **305** responds to commands from the command block **304**, and selectively connects an electrode **212**, **214**, **216**, **218** with conductor S1 or conductor S2.

Circuitry may also be provided that permits IC **301** to send messages back along conductors S1, S2 to system **101** (FIG. **1**).

The data/clock recovery circuitry **303** and the command interpretation circuitry **304** may be the circuitry set forth in international patent publication number WO 2007/075974 or in other patent documents listed above that are incorporated by reference herein.

Default-Mode Operation. In one embodiment, the integrated circuits are configured to be operable in a default mode, e.g., where the circuits are employed in electrode assemblies on a lead, such as a multi-electrode lead (MEL). In such an embodiment, the circuits include a default-mode functional block, which enables the circuit and assembly coupled thereto to operate in a default mode without the electrodes being first powered up and configured. As such, in these embodiments a device configuration provided by said integrated circuit is functional without power being applied to said integrated circuit. This default-mode operation allows an implantable medical device, such as a pacemaker, to operate without consuming extra power for electrode configuration. Furthermore, the default-mode operation allows the MEL to easily interoperate with conventional pacing systems. In such embodiments, the integrated circuit may have a functional block that enables default operation, e.g., as described above.

In certain embodiments, the circuit is configured to have a default configuration connecting one supply terminal to one or more effectors upon power up of said circuit. As such, in these embodiments, upon power up of the circuit, the circuit assumes a default configuration with respect to one or more effectors that are coupled to the circuit, without receiving any configuration data from a remote source.

Discussing this function in greater detail, embodiments of the present invention provide implantable devices, such as satellite units of a multi-electrode lead (MEL) that are operable in a default mode. Such devices include an integrated circuit which is configured such that it is operational upon power up whether or not it receives configuration data following power up. For example, a pacemaker lead of the present invention can operate in a default mode after it is coupled to a pacemaker can, regardless of whether it receives electrode configuration signals from the pacemaker can. In the default mode, a pacemaker lead can provide pacing functions in response to pacing signals that fall within an accepted range. The ranges of signals that are accepted by a pacemaker lead are broad enough to include pacing signals generated by many different models of pacemaker cans. As such, pacemaker leads of the present invention are not limited to being used with only one pacemaker can model or one class of pacemaker cans made by a particular manufacturer.

The present invention provides the ability to replace the preexisting can with one from a wide variety of makes and models, should the need arise. This can be accomplished while using the existing pacemaker leads. This is desirable over performing an additional surgical procedure to replace the preexisting pacemaker leads. It would be desirable if an implanted pacemaker lead could respond to pacing signals generated by one pacemaker model or a class of pacemaker models made by any manufacturer.

Pacemaker leads can include one or more integrated circuit chips. Each of the chips can include a set of switches (e.g., 4 switches). Each of the switches couple or decouple an anode wire or a cathode wire in the lead to an electrode. The switches are typically implemented by a set of transistors according to any convenient circuit design techniques.

A pacemaker lead of the present invention is connected to a pacemaker can. The pacemaker lead is operable in a default mode. In the default mode, the switches in the integrated circuit chips remain in or switch to a default configuration. When the switches are in the default configuration, one or more of the electrodes are coupled to the anode wire and/or the cathode wire. In one approach, the switches in one or more chips can be switched to couple a corresponding electrode to an anode wire or a cathode wire. The switches can also decouple a corresponding electrode from both the anode wire and the cathode wire so that the pacemaker cannot send current to that electrode. Thus, each of the switches can be placed in one of three states: decoupled, coupled to the anode wire, or coupled to the cathode wire.

Turning momentarily to FIG. **9**, what is shown is a pacemaker lead **951** which connects to a pacemaker can at end **952**. Disposed at the distal end of lead **951** (the end furthest from the end **952**) is chip **956**. Next is chip **955**, then chip **954**, and finally chip **953** closest to the pacemaker can. (This example shows four chips and thus four satellites, but other numbers may be employed.)

Each chip is connected to electrodes. For example chip **953** is connected to electrodes **957**, chip **954** is connected to electrodes **958**, chip **955** is connected to electrodes **959**, and chip **956** is connected to electrodes **960**.

Within each chip are semiconductor switches (omitted for clarity in FIG. **9**) which can selectively connect a particular electrode to conductor S1 or to conductor S2, or can leave the electrode at a high impedance relative to conductors S1 and S2. Each electrode has two such switches (one coupled to S1 and the other coupled to S2), and thus in this embodiment each chip has four electrodes, so that each chip contains eight such switches. In the exemplary embodiment of lead **951**, which has four chips, there are thus thirty-two such switches.

In an exemplary embodiment the chips disposed at **953**, **954**, **955**, **956** are not identical in their default function. A first type of chip is a chip which, in default, connects all of its electrodes to the cathode (S1) conductor. A second type of chip, in default, connects all of its electrodes to the anode (S2) conductor. A third type of chip, in default, does not connect its electrodes to either of the conductors.

In the embodiment of FIG. **9**, the chip **956** is of the first type (here called "c0") namely with a default connection to the cathode (S1) conductor. The chip **955** is of the second type (here called "a1") namely with a default connection to the anode (S2) conductor. Each of chips **954**, **953** is of the third type (here called "s") which in default does not connect its electrodes to either conductor.

With a legacy pacemaker sending a pulse in a single-wire way (using body tissue as a return for a pulse emitted on the S1 conductor) then the only active electrodes **960** are those at the distal satellite.

With a legacy pacemaker sending a pulse in a two-wire way (on conductors S1 and S2) then the active electrodes are those at **959** (coupled with the S2 conductor) and those at **960** (coupled with the S1 conductor).

Some types of pacemaker cans are able to generate configuration signals that can control the states of the switches in the integrated circuit chips that are in an implantable pacemaker lead. These types of pacemaker cans are able to change

the states of the switches in order to stimulate any of the electrodes in the lead in any desired pacing configuration.

However, other types of pacemaker cans cannot generate configuration signals for controlling the states of the switches. According to the present invention, one or more of the electrodes are coupled to the anode and/or cathode wire in a default mode. Therefore, a pacemaker can that is not able to generate configuration signals for changing the states of the switches is still able to send current to at least one of the electrodes in a default mode. The default configuration of the switches allows any pacemaker can that is able to generate pacing signals within an accepted range to stimulate the cardiac tissue and provide at least a basic pacing function.

According to some embodiments of the present invention, an implantable pacemaker lead is already in a functional default mode before the lead is coupled to a pacemaker can. According to other embodiments of the present invention, an implantable pacemaker lead enters a functional default mode after the lead is coupled to a pacemaker can, and the power supply voltage reaches or exceeds a predefined threshold voltage. As mentioned above in connection with FIG. **9**, the integrated circuit chips on a pacemaker lead can be classified as three types of default mode chips: anode default, cathode default, and off default. Anode default chips contain switches that couple one or more electrodes to the anode wire in default mode. The DC lead impedance for an anode default chip can be, for example, in the range of about 20 to about 225Ω, such as from about 112 to about 225Ω, such as about 120Ω.

Cathode default chips contain switches that couple one or more electrodes to the cathode wire in default mode. The DC lead impedance for a cathode default chip can be, for example, in the range of about 15 to about 80Ω, such as from about 20 to about 80Ω, including about 40Ω. If the pulse amplitudes of the pacing signals are increased, the lead impedances are reduced.

Chips that are off by default contain switches that disconnect all of their electrodes from the anode and cathode wires. Chips that are off by default can be, for example, in the range of about a megohm impedance until turned on using a pacemaker can.

A pacemaker lead of the present invention can have integrated circuit chips with any number of switches that are coupled to a corresponding number of electrodes. For example, in one instance, electrode configuration can be set to provide the patient an effective therapeutic procedure. In another instance, the electrode configuration can be reset to provide the same patient a more effective therapeutic procedure.

Power generation. Returning to FIG. **3**, the power extraction or power generation circuitry **302** is shown. conductors S**1** and S**2** receive power from outside of the chip **301**. The power extraction circuitry **302** has the task of developing an appropriate power supply for use within the chip **301**, here with conductors **308** and **306** arbitrarily denoted as Vhigh and Vlow respectively.

Electrode switching to S**2** conductor. Returning to FIG. **3**, the switching circuitry **305** is shown. conductors S**1** and S**2** receive signals from outside of the chip **301**. The switching circuitry **305** provides a tri-state driver for each electrode **212**, **214**, **216**, **218**. By "tri-state driver" is meant that a particular electrode might be connected to conductor S**1** or to conductor S**2** or might be at a high impedance relative to both of conductors S**1** and S**2** ("floating"). The drivers are controlled by control lines **307** (FIG. **3**) from the command interpretation circuitry **304**.

FIG. **8** details a portion of the switching circuitry **305** in a system according to the invention. Electrode **212** is connected by a line O with switches O**2** and O**1** which together comprise a tri-state driver. Electrode **214** is connected by a line P with switches P**2** and P**1** which together comprise a tri-state driver. Electrode **216** is connected by a line L with switches L**2** and L**1** which together comprise a tri-state driver. Finally, electrode **218** is connected by a line F with switches F**2** and F**1** which together comprise a tri-state driver.

In FIG. **8**, each tri-state driver is controlled by control lines **307**, the details of which are omitted for clarity in FIG. **8**. As with any tri-state driver, it is important that at most one of the switches be "on" at a particular time. Stated differently, it should never happen that both switches are on at the same time. This, for example, switches **02** and **01** should never be simultaneously "on".

Coping with severely limited voltage. One of the many challenges facing the designer of a lead is, as mentioned above, the problem that the designer is not permitted to make very many assumptions about the power provided to the lead by the external equipment such as a pacemaker. The power may be of very limited voltage, perhaps as little as one volt. Yet the main circuitry of the chip in each satellite of the lead is likely to require about two volts to carry out its tasks.

Turning to FIG. **4**, what is seen is a classic flying-capacitor voltage doubler **421** as is well known in the art. A voltage input **422** is provided to the doubler **421**. The output **423** is shown. Capacitor **424** is connected by double-pole double-throw switch **426** as will be discussed in some detail. DPDT switch **426** is controlled by timing signal or signals **425**.

In a first phase, the switch **426** connects the capacitor **424** between input **422** and ground, with the top of the capacitor connected to the input **422** and the bottom of the capacitor connected to ground. This charges up the capacitor **424**.

In a second phase, the switch **426** connects the top of the capacitor to the output **423**, and connects the bottom of the capacitor to the input **422**.

In this way the voltages are "added up". The voltage at the input (say, 1 volt) is added to the voltage stored in the capacitor (also 1 volt, having been charged during the first phase). The sum, two volts, is delivered to the output **423**.

FIG. **5** shows in schematic detail a voltage doubler **521** as employed in the apparatus according to the invention. Input **522** may be seen, as well as output **523**. Capacitor **524** is shown. Transistor switches **534**, **532**, **530**, and **528** are shown, and they provide the function described in FIG. **4** by switch **426**. The transistor switches are turned on and off by timing signals **533**, **531**, **529**, and **527**.

In a typical embodiment the timing signals cycle at a megahertz or so. Such a frequency permits minimizing the size of the capacitors **424** (FIG. **4**) and **524** (FIG. **5**). If much lower frequencies had been used, it would have been necessary to make the capacitors larger, and this is not easy to do in an integrated circuit of limited size such as is being discussed herein.

FIG. **6** shows a composite voltage doubler **621** composed of voltage doublers **622**, **623** excited out of phase with each other, so as to provide better power generation. Input **625** and output **624** are shown. Timing signals **626**, **627** are provided to the doublers **622** and **623** respectively. The timing signals are, in this embodiment, 180 degrees out of phase with each other. In this way, the two doublers **622** and **623** fill in each others' gaps, providing double the bandwidth of a single doubler **622** or **623** taken alone.

Yet another challenge, as mentioned above, is that the designer of the lead is required to provide fully functioning chips within only a few tens of microseconds of the initial arrival of power at the lead. It turns out that a single voltage

doubler (and its associated timing circuitry) cannot reliably "settle" quickly enough into generation of the needed voltage levels.

FIG. **7** shows cascaded voltage doublers according to the invention. A voltage input **722** is shown, which is provided to first timing circuitry **724**, to first doubler **725**, and to second doubler **730**. First timing circuitry **724** provides timing signals **728** to first doubler **725**.

First doubler **725** provides doubled voltage to second timing circuitry **726**. Second timing circuitry **726** provides timing signals **729** to second doubler **730**. Second doubler **730** has output **723**.

First doubler **725**, together with first timing circuitry **724**, is designed to "settle" very quickly, which it is able to do because it does not need to generate a lot of power. It only needs to generate enough power to give stable operation to second timing circuitry **729** (and it need not generate enough power to power the main functions of the chip).

Second doubler **730**, together with second timing circuitry **729**, is designed so as to be able to generate enough power to power the main functions of the chip.

In a typical embodiment, the power input **722** might be as small as one volt. First timing circuitry **724** is designed to be able to do its job despite having only one volt powering the circuitry.

The output of the first doubler **725** is nominally two volts, and this permits reliable and stable operation of second timing circuitry **726**.

In this way, the composite doubler **721** is able to provide high quality doubled voltage at output **723**, all within only a few tens of microseconds of initial supply of as little as one volt.

In an exemplary embodiment, the first doubler **724** may have a flying capacitor of between about 2 and 3 picofarads, for example about 2.7 picofarads. In the exemplary embodiment, the second doubler **724** may have a flying capacitor of between about 13 and 16 picofarads. Other doublers that do not need to generate very much current may each have a flying capacitor of between about 250 femtofarads and about 300 or 500 femtofarads.

As was mentioned above, one of the challenges facing the designer of a lead according to the invention is that it is often necessary to accommodate any of a variety of legacy or more modern implantable devices. Thus while one implantable device may provide around 1 or 1.1 volts, a different implantable device may provide a higher voltage such as 3 volts, which higher voltage makes it unnecessary to make use of voltage doublers at all.

This it may be described that the doubler is only needed if the input voltage is low. If the input voltage is sufficiently high, then it might be advantageous to bypass or disable the doubler or doublers to prevent an excessively high output voltage from damaging the other internal parts of the integrated circuit. A threshold for bypassing the doubler or doubler might be about 3 volts DC provided at the lead conductor or conductors.

In one exemplary embodiment of the invention, what is described is a lead for use with an implantable device, the lead having at least two satellites at respective distinct positions along its length, the lead having at least two conductors extending along at least part of its length, the conductors extending to and electrically connected to each of the at least two satellites and further extending to an end of the lead for electrical connection to the implantable device. Each satellite comprises at least one respective electrode positioned for contact external to the lead. Each satellite further comprises a respective integrated circuit electrically connected with the at least two conductors and electrically connected with the respective electrode. Each integrated circuit comprises respective first timing circuitry powered from the at least two conductors. Each integrated circuit further comprises a respective first voltage doubler powered from the at least two conductors and switched by the respective first timing circuitry. Each integrated circuit comprises respective second timing circuitry powered from the first voltage doubler. Each integrated circuit further comprises a respective second voltage doubler powered from the at least two conductors and switched by the respective second timing circuitry. Each integrated circuit further comprises a control means controlling connections between the at least one respective electrode and the at least two conductors, the control means powered from the respective second voltage doubler.

There may be a respective third voltage doubler powered from the at least two conductors and switched by the respective second timing circuitry out of phase with respect to the switching of the second voltage doubler, the control means powered from the respective third voltage doubler in addition to the respective second voltage doubler.

The power provided to the control means by the voltage doubler may be about two volts, characterized as being at least 1.8 volts. The power provided to the voltage doubler by the at least two conductors may be about one volt, characterized as being no more than 1.1 volts. The output of the voltage doubler may be stable within about ten or fifteen or twenty microseconds, characterized as being stable within fifty microseconds of the provision of power to the voltage doubler by the at least two conductors.

An exemplary sequence of events is that within each integrated circuit:

- first timing signals are generated drawing upon power from the at least two conductors;
- a voltage is doubled from the at least two conductors, the doubling switched by the respective first timing signals, yielding a first doubled voltage;
- second timing signals are generated drawing upon power from the first voltage doubled voltage;
- a voltage is doubled from the at least two conductors, the doubling switched by the respective second timing signals, yielding a second doubled voltage.

The above discussion addresses a typical case where the lead contains two conductors. It will be appreciated, however, that the teachings of the invention are equally available in the case where a lead has only one conductor, the remainder of the conduction path being through body tissue to a connection point at the implantable device.

The above discussion uses the term "voltage doubler" as a convenient way to describe the approach that is employed to address some of the challenges faced by designers in the area being discussed. The more general term "charge pump" is perhaps a clearer term to describe the approaches set forth for addressing some of the challenges.

Those skilled in the relevant art will have no difficulty whatsoever devising myriad obvious improvements and variants of the apparatus and methods without undue experimentation, all of which improvements and variants are intended to be encompassed within the claims which follow.

The invention claimed is:

1. A lead for use with an implantable device, the lead having at least two satellites formed along with its length, the lead having at least one conductor extending along at least part of its length, the at least one conductor extending to and electrically connected to each of the at least two satellites and further extending to an end of the lead for electrical connection to the implantable device, with each satellite comprising:

at least one electrode positioned for contact external to the lead; and

an integrated circuit electrically connected with the at least one conductor and electrically connected with the at least one electrode, the integrated circuit comprising:

a first timing circuitry coupled with the at least one conductor and powered from the at least one conductor;

a first charge pump coupled with the at least one conductor and the first timing circuitry and powered from the at least one conductor and switched by the first timing circuitry;

a second timing circuitry coupled with the first charge pump and powered from the first charge pump;

a second charge pump coupled with the at least one conductor and the second timing circuitry, the second charge pump powered from the at least one conductor and switched by the second timing circuitry;

a third charge pump coupled with the at least one conductor and the second timing circuitry, the third charge pump powered from the at least one conductor and switched by the second timing circuitry out of phase with respect to switching of the second charge pump; and

a control means controlling connections between the at least one electrode and the at least one conductor, the control means coupled with the second charge pump and the third charge pump and powered from the second charge pump and the third charge pump.

2. The lead of claim **1**, wherein the power provided to the control means by the first charge pump is at least 1.8 volts, and wherein the power provided to the first charge pump by the at least one conductor is no more than 1.1 volts.

3. The lead of claim **1** wherein an output of the first charge pump becomes stable within fifty microseconds from an initial provision of power to the first charge pump by the at least one conductor.

4. The lead of claim **1** wherein the first charge pump is disabled or bypassed when power provided to the first charge pump by the at least one conductor is at least 3 volts.

5. The lead of claim **1** wherein the second charge pump is disabled or bypassed when power provided to the second charge pump by the at least one conductor is at least 3 volts.

6. The lead of claim **1** wherein a number of the at least one conductor is one.

7. The lead of claim **1** wherein a number of the at least one conductor is two.

8. The lead of claim **1** wherein a number of the at least one electrode is at least four.

9. The lead of claim **1** wherein a number of the at least one electrode is at least four.

10. A satellite for use with a lead having at least one conductor, the lead for use with an implantable device, the satellite comprising:

at least one electrode positioned for contact external thereto; and

an integrated circuit electrically connected with the at least one conductor and electrically connected with the at least one electrode, the integrated circuit comprising:

a first timing circuitry coupled with the at least one conductor and powered from the at least one conductor;

a first charge pump coupled with the at least one conductor and the first timing circuitry and powered from the at least one conductor and switched by the first timing circuitry;

a second timing circuitry coupled with the first charge pump and powered from the first charge pump;

a second charge pump coupled with the at least one conductor and the second timing circuitry, the second charge pump powered from the at least one conductor and switched by the second timing circuitry;

a third charge pump coupled with the at least one conductor and the second timing circuitry, the third charge pump powered from the at least one conductor and switched by the second timing circuitry out of phase with respect to switching of the second charge pump; and

a control means controlling connections between the at least one electrode and the at least one conductor, the control means coupled with the second charge pump and the third charge pump and powered from the second charge pump and the third charge pump.

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