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(54) **DEVICE WITH CAPABILITY OF PROCESSING FFT RADIX 2 BUTTERFLY OPERATION AND OPERATION METHOD THEREOF**

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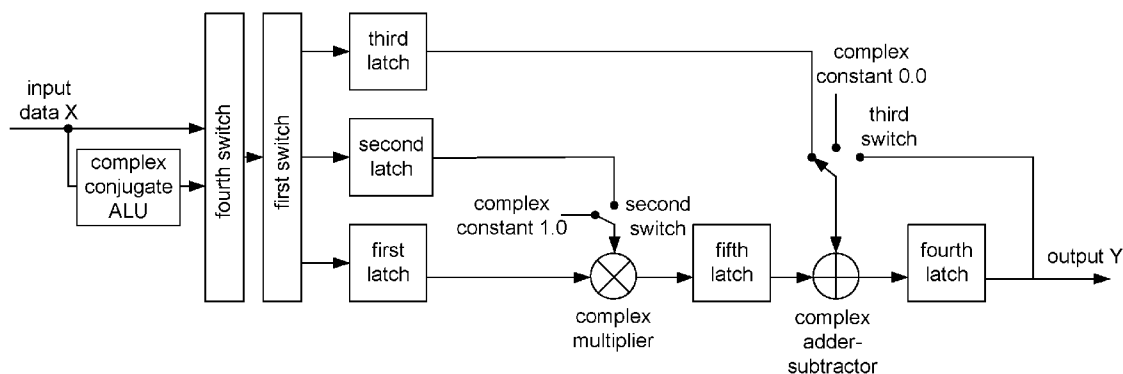
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(57) **ABSTRACT**

The disclosure provides a device with a capability of processing a Fast Fourier Transform Algorithm (FFT) radix 2 butterfly operation and an operation method thereof, the device at least includes a latch, a complex multiplier, a complex adder-subtractor, a switch and a complex conjugate Arithmetic Logical Unit (ALU). The complex operation unit of the disclosure has a simple structure. The parallel processing array composed of the complex operation unit has the capability of efficiently processing vectors and the FFT operation.

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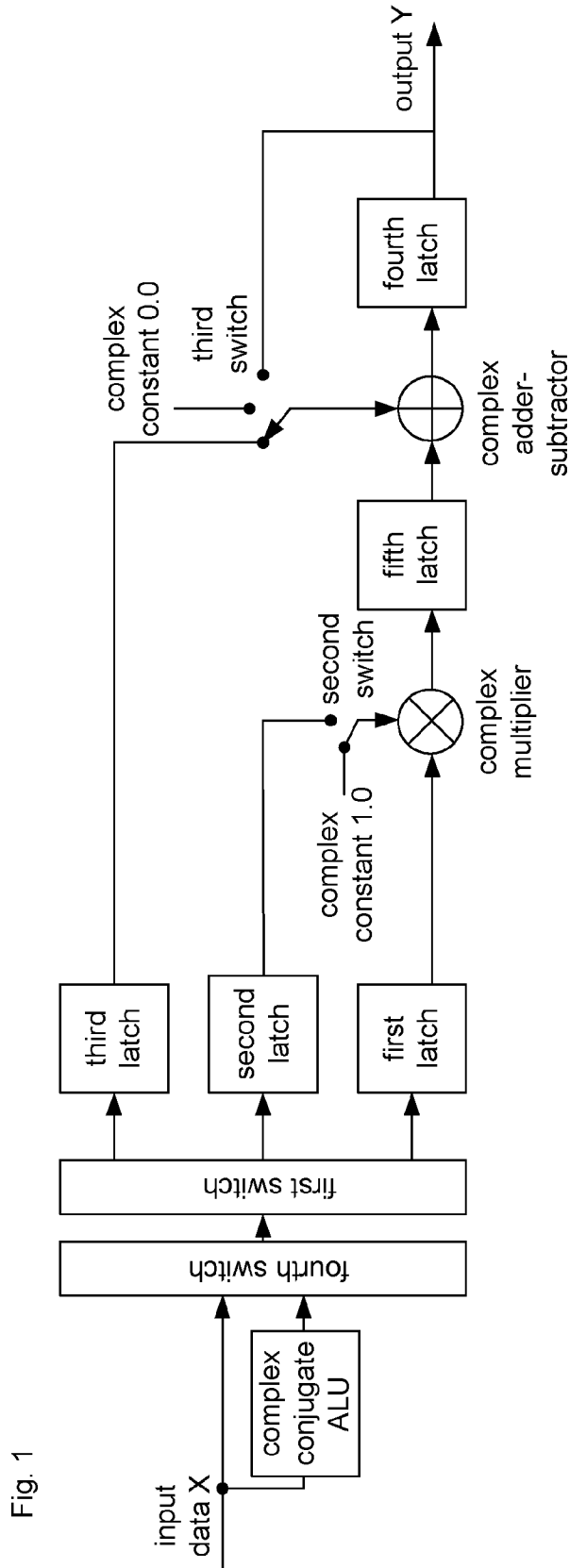
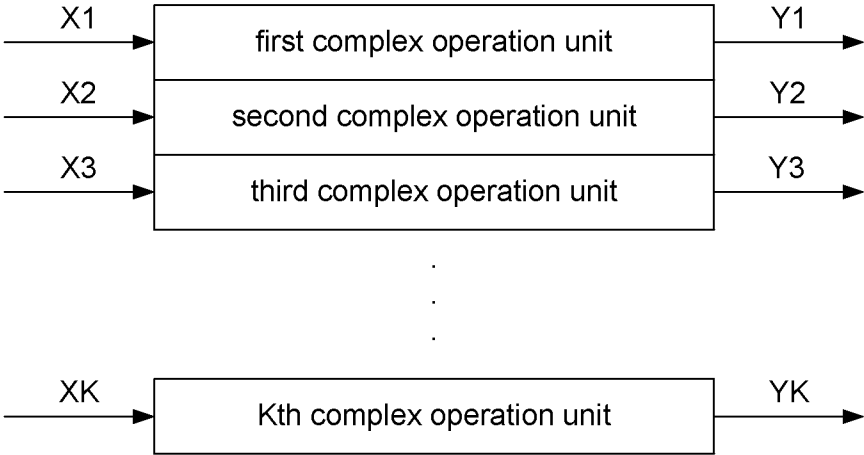


Fig. 1

Fig. 2



**DEVICE WITH CAPABILITY OF  
PROCESSING FFT RADIX 2 BUTTERFLY  
OPERATION AND OPERATION METHOD  
THEREOF**

TECHNICAL FIELD

**[0001]** The disclosure relates to large scale digital signal processing technique, in particular to a device with a capability of processing a Fast Fourier Transform (FFT) radix 2 butterfly operation and an operation method thereof.

BACKGROUND

**[0002]** Large scale digital signal processing technique, especially array digital signal and FFT processing technique requires a processor platform to provide a strong capability of processing parallel. Such parallel array processor with a capability of processing large scale digital signal has more extensive application in the field of large scale digital signal processing.

**[0003]** In the digital signal processing field, a large scale parallel operation array is used widely with the constant increases of signal processing speed and complexity and cost performance ratio of the processor. In particular in the field of wireless communications, a lot of applications of new base-band technology, such as Multiple-Input Multiple-Output (MIMO), antenna array beam forming technology, multi-user interference counteract (Turbo-MIMO), puts enormous pressure on the digital signal processing platform. In the circumstances, the parallel processing array shows its strong performance on high speed signal processing.

SUMMARY

**[0004]** Accordingly, the main purpose of the disclosure is to provide a device with a capability of processing an FFT radix 2 butterfly operation and an operation method thereof, which have a capability of efficiently processing vectors and strong FFT radix 2 butterfly operation.

**[0005]** To this end, the technical scheme of the disclosure is realized as follows. A device with a capability of processing a Fast Fourier Transform (FFT) radix 2 butterfly operation includes: a latch, a complex multiplier, a complex adder-subtractor, a switch and a complex conjugate Arithmetic Logical Unit (ALU), wherein:

**[0006]** the complex conjugate ALU is configured to convert input data X into a conjugate of the input data X;

**[0007]** a fourth switch is configured to select the input data X or the conjugate of the input data X to output the selected data;

**[0008]** a first switch is configured, under control of an external control signal, to send the input data X or the conjugate of the input data X to one of a first latch, a second latch and a third latch in each clock to temporarily store the sent data;

**[0009]** the complex multiplier is configured to have two inputs of which one is from the first latch and another is from a second switch, wherein data generated by the complex multiplier is output to a fifth latch to be latched;

**[0010]** the second switch is configured, under control of an external control signal, to input output data of the second latch or a complex constant 1.0 to the complex multiplier;

**[0011]** the complex adder-subtractor is configured to have two inputs of which one is from the fifth latch and another is from a third switch;

**[0012]** the third switch is configured to have three inputs which respectively are from output of the third latch, output of a fourth latch and a complex constant 0.0, and the third switch is configured, under control of an external control signal, to select one input to transmit the selected input to the complex adder-subtractor; and

**[0013]** the fourth latch is configured to store output of the complex adder-subtractor, and to form an accumulator together with the complex adder-subtractor; wherein output of the fourth latch is output Y of the device.

**[0014]** At least two devices with a capability of processing an FFT radix 2 butterfly operation may form a parallel complex operation array.

**[0015]** An operation method of a device with a capability of processing a Fast Fourier Transform (FFT) radix 2 butterfly operation includes:

**[0016]** performing a single-operand operation using the above device.

**[0017]** The single-operand operation may include: a traversing operation, a single-operand complex add or subtraction operation.

**[0018]** The method may further include: performing a double-operand operation using the device.

**[0019]** The double-operand operation may include: a double-operand add or subtraction operation, a double-operand multiplication.

**[0020]** The method may further include: performing a triple-operand operation using the device.

**[0021]** The triple-operand operation may include: a triple-operand multiply-add or multiply-subtraction operation, and a triple-operand FFT radix 2 butterfly operation.

**[0022]** A parallel complex operation array is formed when there are two or more devices; and the method may further include: performing addition and subtraction of two K dimension complex vectors and elements multiplication operations, multiplication of a  $K \times K$  matrix by a  $K \times 1$  vector, a  $2K$  point FFT radix 2 butterfly operation by using K devices, wherein K is a number of the devices.

**[0023]** It can be seen from the above solutions, the complex operation unit of the disclosure has a simple structure, and the parallel processing array composed of the complex operation unit has the capability of efficiently processing vectors and an FFT radix 2 butterfly operation.

BRIEF DESCRIPTION OF THE DRAWINGS

**[0024]** FIG. 1 shows a schematic diagram of a structure of a device with a capability of processing an FFT radix 2 butterfly operation according to the disclosure; and

**[0025]** FIG. 2 shows a schematic diagram of an operation array composed of a device with a capability of processing an FFT radix 2 butterfly operation according to the disclosure.

DETAILED DESCRIPTION

**[0026]** FIG. 1 shows a schematic diagram of a structure of a device with a capability of processing an FFT radix 2 butterfly operation according to the disclosure. As shown in FIG. 1, the device at least includes a latch, a complex multiplier, a complex adder-subtractor, a switch and a complex conjugate Arithmetic Logical Unit (ALU). The disclosure does not limit an input and output bit width of each of the latch, the complex multiplier, the complex adder-subtractor, the switch and the complex conjugate ALU. Specific description may be as follows.

**[0027]** The device with a capability of processing an FFT radix 2 butterfly operation shown in FIG. 1 is also known as a complex operation unit which may be a fixed point operation unit or a floating point operation unit. The complex operation unit has input data X.

**[0028]** The complex conjugate ALU outputs a conjugate value of X. A fourth switch S4 selectively inputs the input data X or the conjugate value of X, and is connected to three latches (i.e., a first latch, a second latch and a third latch) through a first switch S1.

**[0029]** The first, second and third latches are configured, under the control of the first switch S1, to provide the input data X to one latch of them to temporarily store the input data X.

**[0030]** The complex multiplier has two inputs of which one is from the first latch and another is from a second switch S2.

**[0031]** The second switch S2 is configured, under the control of an external control signal, to input output data of the second latch or a complex constant 1.0 to the complex multiplier. Output data of the complex multiplier is latched by a fifth latch.

**[0032]** The complex adder-subtractor has two inputs of which one is from the fifth latch and another is from a third switch S3.

**[0033]** The third switch S3 has three inputs which respectively are from output of the third latch, output of a fourth latch and a complex constant 0.0. The switch S3 is configured, under the control of an external control signal, to select one input to transmit the selected input to the complex adder-subtractor. The principle for implementing external control is as follows: if an operation does not include an add operation, the third switch S3 selects the complex constant 0.0, i.e., to add 0.0; if the operation includes an add operation, the third latch is selected; if the operation needs to perform an accumulation operation, the fourth latch is selected.

**[0034]** The fourth latch is configured to store output of the complex adder-subtractor, to form an accumulator together with the complex adder-subtractor, and to be cooperated with the complex multiplier to perform a complex MAC operation.

**[0035]** The disclosure does not limit processed data and bit width thereof which may be a floating point or a fixed point.

**[0036]** Specifically, a single-operand operation performed by the complex ALU is as follows.

**[0037]** traversing: the input data X is directly output. As shown in FIG. 1, a data path is: input X→the fourth switch S4→the first switch S1 the first latch→the complex multiplier (multiply by the complex constant 1.0)→the fifth latch→the complex adder-subtractor (add the complex constant 0.0)→the fourth latch→output Y.

**[0038]** A single-operand complex conjugate operation: it means that a conjugate operation is performed on an external complex. As shown in FIG. 1, a data path is: input X→the complex conjugate ALU→the fourth switch S4→the first switch S1→the first latch→the complex multiplier (multiply by the complex constant 1.0)→the fifth latch→the complex adder-subtractor (add the complex constant 0.0)→the fourth latch→output Y.

**[0039]** A single-operand complex add (subtraction) operation: it means that an external complex adds (or subtracts) data in the internal fourth latch. As shown in FIG. 1, a data path is: input X→the fourth switch S4→the first switch S1 the first latch→the complex multiplier (multiply by the complex

constant 1.0)→the fifth latch→the complex adder-subtractor (add or subtract data stored in the fourth latch)→the fourth latch→output Y.

**[0040]** A double-operand operation performed by the complex ALU is as follows.

**[0041]** A double-operand complex add (subtraction) operation: it means that two operands pass the fourth switch and the first switch in adjacent two periods and are respectively transmitted to the first latch and the third latch. A data path is as follows.

**[0042]** At first, input X1→the first latch; input X2→the third latch;

**[0043]** Next, the first latch→the complex multiplier (multiply by the complex constant 1.0)→the fifth latch→the complex adder-subtractor (add or subtract output data of the third latch)→the fourth latch→output Y.

**[0044]** An output passing rate of the double-operand complex add (subtraction) operation is that one operation is performed in every two periods.

**[0045]** A double-operand complex multiplication: it means that two operands pass the fourth switch and the first switch in adjacent two periods and are respectively transmitted to the first latch and the second latch. A data path is as follows.

**[0046]** At first, input X1→the first latch; input X2→the second latch;

**[0047]** Next, the first latch→the complex multiplier (multiply by data temporarily stored in the second latch)→the fifth latch→the complex adder-subtractor (add the complex constant 0.0)→the fourth latch→output Y.

**[0048]** An output passing rate of the double-operand complex multiplication is that one operation is performed in every two periods.

**[0049]** A triple-operand operation performed by the complex ALU is as follows.

**[0050]** A triple-operand complex multiply-add (or multiply-subtraction) operation, i.e.,  $(A*B+C)$ , in which two operands A and B are from external and the operand C is from the internal fourth latch. The two operands A and B pass the fourth switch and the first switch in adjacent two periods and are respectively transmitted to the first latch and the second latch. A data path is as follows.

**[0051]** At first, input A→the first latch; input B→the second latch;

**[0052]** Next, the first latch→the complex multiplier (multiply by data temporarily stored in the second latch)→the fifth latch→the complex adder-subtractor (add or subtract data temporarily stored in the fourth latch)→the fourth latch→output Y.

**[0053]** An output passing rate of the triple-operand complex multiply-add (or multiply-subtraction) operation is that one operation is performed in every two periods.

**[0054]** Another triple-operand complex multiply-add (or multiply-subtraction) operation, i.e.,  $(A*B+C)$ , in which each operand A, B and C is from external. Three operands A, B and C pass the fourth switch and the first switch in adjacent two periods and are respectively transmitted to the first latch, the second latch and the third latch. A data path is as follows.

**[0055]** At first, input A→the first latch; input B→the second latch; input C→the third latch;

**[0056]** Next, the first latch→the complex multiplier (multiply by data temporarily stored in the second latch)→the fifth latch→the complex adder-subtractor (add or subtract data temporarily stored in the third latch)→the fourth latch→output Y.

**[0057]** An output passing rate of this triple-operand complex multiply-add (or multiply-subtraction) operation is that one operation is performed in every three periods.

**[0058]** Triple-operand FFT radix 2 butterfly operation, i.e.,  $Z0=a+W*b$  or  $Z1=a-W*b$ . Each operand a, b and W is from external. Three operands a, b and W pass the fourth switch and the first switch in adjacent two periods and are respectively transmitted to the first latch, the second latch and the third latch. A data path is as follows.

**[0059]** At first, input b→the first latch; input W→the second latch; input a→the third latch;

**[0060]** Next, the first latch→the complex multiplier (W multiply by b, i.e.,  $W*b$ )→the fifth latch;

**[0061]** A data path for  $Z0=a+Wb$  is as follows: →the complex adder-subtractor (add output data of the third latch, i.e.,  $a+W*b$ )→the fourth latch→output Y.

**[0062]** A data path for  $Z0=a-Wb$  is as follows: the complex adder-subtractor (subtract output data of the fifth latch from output data of the third latch, i.e.,  $a-W*b$ )→the fourth latch→output Y.

**[0063]** An output passing rate of the triple-operand FFT radix 2 butterfly operation is that one FFT radix 2 butterfly operation is performed in every three periods.

**[0064]** The following complex operations may be performed through the complex operation unit shown in FIG. 1: complex conjugate; complex A adds/subtracts complex B; complex A multiplies by complex B; complex A multiplies by complex B and then adds/subtracts complex C; Radix 2 FFT butterfly operation, complex A, complex B and complex C are input data.

**[0065]** Several complex operation units (such as K units) shown in FIG. 1 may form a parallel complex operation array (K array for short). The K array may be used as an ALU for a vector processor or an array processor, in which the K array may have a capability of running complex addition or multiplication K times in each clock cycle. The K array may have a capability of running the FFT radix 2 butterfly operation K times in three clocks.

**[0066]** FIG. 2 shows a schematic diagram of an operation array composed of a device with a capability of processing an FFT radix 2 butterfly operation according to the disclosure.

**[0067]** As shown in FIG. 2, a K array composed of K complex operation units may perform vector, an FFT operation and a Discrete Fourier Transform (DFT) operation. Hereinafter, the device will be described in detail with some examples.

**[0068]** For addition and subtraction of two K dimension complex vectors and elements multiplication operations, the K array has a capability of processing one operation in every two periods.

**[0069]** For multiplication of a  $K*K$  matrix by a  $K*1$  vector, the K array has a capability of processing one operation in every  $(K+1)$  periods.

**[0070]** For a  $2K$  point FFT operation, the K array has a capability of processing one operation in every  $3 \log_2 2K$  periods.

**[0071]** K common multiple vector, matrix or FFT may be divided into sub-vectors, sub-matrixes or sub-modules by taking K as a unit, then each of sub-vectors, sub-matrixes or sub-modules is operated respectively, and then results are put together.

**[0072]** For K common measure vector, matrix or FFT, the K array may perform plurality of operations in parallel, simultaneously.

**[0073]** For other cases, a plurality of manners such as partition or merge may be used. The principle is to take full advantage of resource of each operation unit of the K array.

**[0074]** It is obvious for those skilled in the art to use the K array composed of K complex operation units to perform operations based on the complex operation unit shown in FIG. 1, which will not be further elaborated.

**[0075]** The complex operation unit of the disclosure has a simple structure. The parallel processing array composed of the complex operation unit has the capability of efficiently processing vectors and the FFT operation.

**[0076]** Since the FFT operation is widely used in digital signal processing, in particular to the fourth generation mobile communication based on the Orthogonal Frequency Division Multiplexing (OFDM) technique, such as a Long Term Evolution (LTE) system and a Worldwide Interoperability for Microwave Access (WiMAX) system, the capability of processing FFT directly affects application cost of the whole system, therefore, the operation array composed of the complex operation unit with a capability of processing an FFT radix 2 butterfly operation according to the disclosure may directly be used to construct a high performance baseband processor.

**[0077]** Since the complex operation unit according to the disclosure has programmability, the parallel array processor composed of the complex operation unit may be used as a wireless multimode soft baseband platform for covering a plurality of wireless standards such as LTE, WiMAX, WCDMA, TD-SCDMA, CDMA2000 and the like.

**[0078]** Although preferable embodiments of the disclosure have been described for the sake of illustration, those skilled in the art will note that it is possible to make various modifications, additions and replacements. Therefore, the protection scope of the disclosure is not limited to the above embodiments.

What is claimed is:

1. A device with a capability of processing a Fast Fourier Transform (FFT) radix 2 butterfly operation, comprising a latch, a complex multiplier, a complex adder-subtractor, a switch and a complex conjugate Arithmetic Logical Unit (ALU), wherein:

the complex conjugate ALU is configured to convert input data X into a conjugate of the input data X;

a fourth switch is configured to select the input data X or the conjugate of the input data X to output the selected data;

a first switch is configured, under control of an external control signal, to send the input data X or the conjugate of the input data X to one of a first latch, a second latch and a third latch in each clock to temporarily store the sent data;

the complex multiplier is configured to have two inputs of which one is from the first latch and another is from a second switch, wherein data generated by the complex multiplier is output to a fifth latch to be latched;

the second switch is configured, under control of an external control signal, to input output data of the second latch or a complex constant 1.0 to the complex multiplier;

the complex adder-subtractor is configured to have two inputs of which one is from the fifth latch and another is from a third switch;

the third switch is configured to have three inputs which respectively are from output of the third latch, output of

- a fourth latch and a complex constant 0.0, and the third switch is configured, under control of an external control signal, to select one input to transmit the selected input to the complex adder-subtractor; and
- the fourth latch is configured to store output of the complex adder-subtractor, and to form an accumulator together with the complex adder-subtractor; wherein output of the fourth latch is output Y of the device.
2. The device according to claim 1, wherein at least two devices with a capability of processing an FFT radix 2 butterfly operation form a parallel complex operation array.
  3. An operation method of a device with a capability of processing a Fast Fourier Transform (FFT) radix 2 butterfly operation, comprising:
    - performing a single-operand operation using the device according to claim 1.
  4. The method according to claim 3, the single-operand operation comprises: a traversing operation, a single-operand complex add or subtraction operation.

5. The method according to claim 3, further comprising: performing a double-operand operation using the device.
6. The method according to claim 5, the double-operand operation comprises: a double-operand add or subtraction operation, a double-operand multiplication.
7. The method according to claim 5, further comprising: performing a triple-operand operation using the device.
8. The method according to claim 7, the triple-operand operation comprises: a triple-operand multiply-add or multiply-subtraction operation, and a triple-operand FFT radix 2 butterfly operation.
9. The method according to claim 5, wherein a parallel complex operation array is formed when there are two or more devices; the method further comprising:
  - performing addition and subtraction of two K dimension complex vectors and elements multiplication operations, multiplication of a K\*K matrix by a K\*1 vector, a 2K point FFT radix 2 butterfly operation by using K devices, wherein K is a number of the devices.

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