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Shen

(54) METHOD AND APPARATUS FOR PROCESSING BASEBAND UPLINK AND DOWNLINK SUB-FRAMES

(75) Inventor: **Chengke Shen**, Shenzhen (CN)

(73) Assignee: **ZTE Corporation**, Shenzhen, Guangdong (CN)

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(57) **ABSTRACT**

The present disclosure provides a method and an apparatus for processing baseband uplink and downlink sub-frames. The method is for serial processing of uplink sub-frames and downlink sub-frames at a base station side of an LTE-TDD system, wherein a length of time slots for processing each sub-frame meets formulae

$$\begin{cases} 3x + 2y + T_{L2} \le 5.0 \text{ ms} \\ 2x + y \le 4 - 2T_a - T_d. \end{cases}$$

By serial processing of the uplink and downlink sub-frames according to the present invention, more abundant processing time may be obtained. In other words, the baseband processor can operate at a lower speed, thus reducing an idle rate of the baseband processor and improving a resource utilization of the processor.

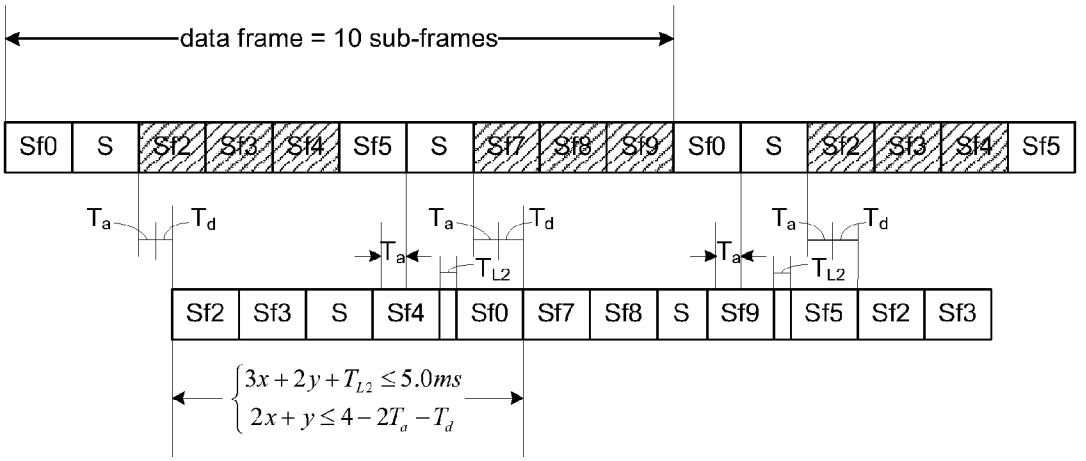


Fig.1

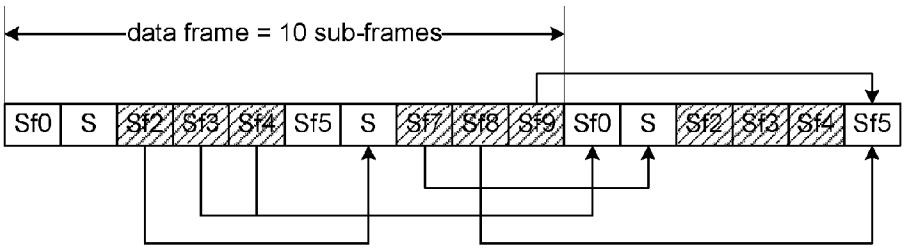


Fig.2

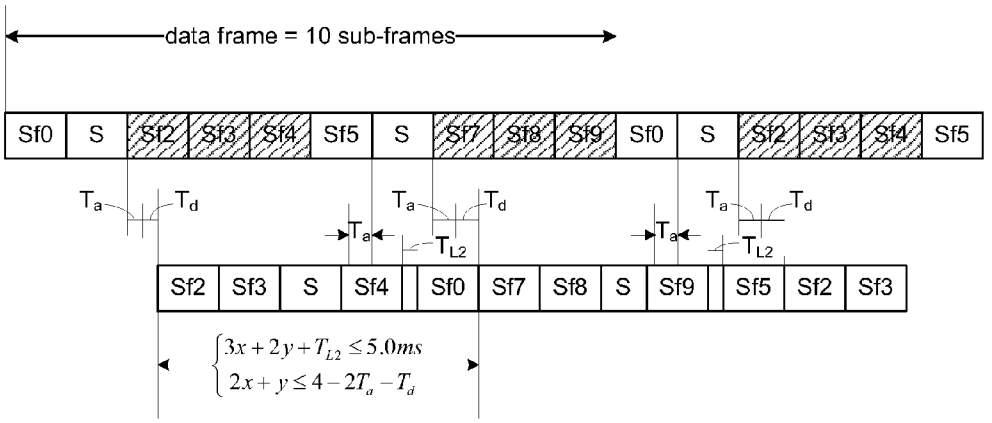


Fig.3

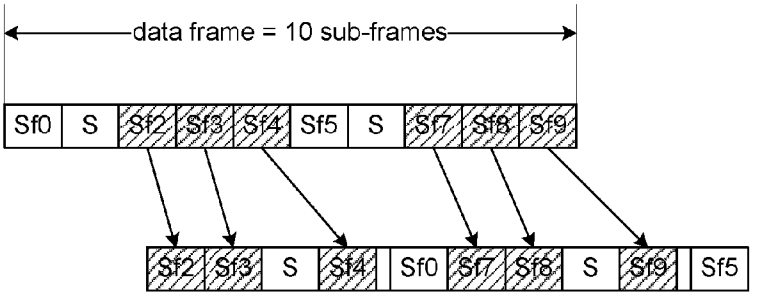
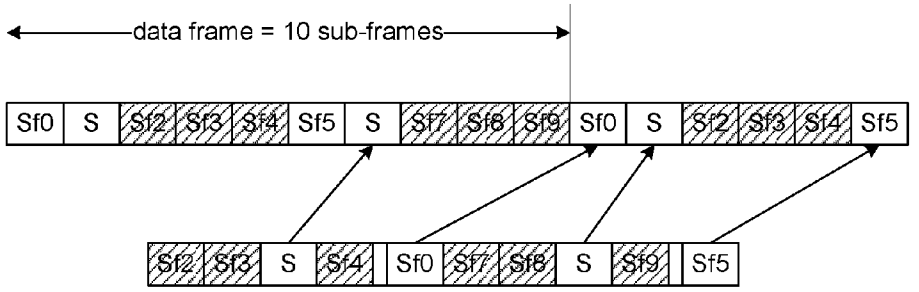


Fig.4


data frame = 10 sub-frames
Sf0
S
Sf2
Sf3
Sf4
Sf5
S
Sf7
Sf8
Sf9
Sf0
S
Sf2
Sf3
Sf4
Sf5
Sf2
Sf3
S
Sf4
Sf0
Sf7
Sf8
S
Sf9
Sf5

METHOD AND APPARATUS FOR PROCESSING BASEBAND UPLINK AND DOWNLINK SUB-FRAMES

TECHNICAL FIELD

[0001] The present disclosure relates to Long Term Evolution-Time Division Duplex (LTE-TDD) base station system techniques, and in particular to a method and apparatus for processing baseband uplink and downlink sub-frames at an LTE-TDD base station side.

BACKGROUND

[0002] In an LTE-TDD system, time slots of uplink and downlink sub-frames of a Physical Uplink Shared Channel (PUSCH) and a Physical Downlink Shared Channel (PDSCH) are not completely parallel in time. During implementation of an LTE-TDD base station, as the uplink and downlink PUSCH and PDSCH sub-frames are arranged in serial in time, parallel processing at the uplink and downlink, namely, processing the sub-frames according to an order of sub-frames 0, 1, 2, . . . , 9, often leads to an excessively high idle rate of a baseband processor, thus reducing a resource utilization of the processor.

[0003] In order to improve the resource utilization of the processor, the present disclosure adopts a solution of serial processing of the uplink and downlink sub-frames with a same processor (or processor array). For this solution, the method for length allocation and the best arrangement of time slots for processing the uplink and downlink sub-frames in the worst case is given. Relative to the uplink and downlink parallel method, such a serial method may obtain more abundant processing time. In other words, the baseband processor only needs a lower speed.

SUMMARY

[0004] In view of the above, the main objective of the disclosure is to provide a method and apparatus for processing baseband uplink and downlink sub-frames capable of reducing the idle rate of the baseband processor, thereby improving the resource utilization of the processor.

[0005] To achieve this objective, the technical solution of the present disclosure is implemented as follows:

[0006] A method for processing baseband uplink and downlink sub-frames, includes:

[0007] serially processing uplink sub-frames and downlink sub-frames at a base station side of a Long Term Evolution-Time Division Duplex (LTE-TDD) system, wherein a length of time slots for processing each sub-frame meets formulae

$$\begin{cases} 3x + 2y + T_{L2} \le 5.0 \text{ ms} \\ 2x + y \le 4 - 2T_a - T_d, \end{cases}$$

[0008] wherein T_a is a delay in transmission from a designated receiving antenna to a baseband processor, T_d is a delay in initiating baseband sub-frame processing, T_{L2} is a time reserved for MAC layer processing, x represents an allowable length of time slots for processing an uplink sub-frame, and y represents an allowable length of time slots for processing a downlink sub-frame.

[0009] An order of processing arrangement in the serially processing uplink sub-frames and downlink sub-frames may be: a sub-frame 2 of a current frame, a sub-frame 3 of the current frame, a sub-frame 6 of the current frame, a sub-frame 4 of the current frame, a sub-frame 0 of a next frame, a sub-frame 7 of the current frame, a sub-frame 8 of the current frame, a sub-frame 1 of the next frame, a sub-frame 9 of the current frame, and a sub-frame 5 of the next frame,

[0010] wherein a reserved time slot with a length of at least T_{L2} may be inserted between the sub-frame 4 of the current frame and the sub-frame 0 of the next frame, and the reserved time slot with a length of at least T_{L2} may be inserted between the sub-frame 9 of the current frame and a downlink sub-frame 5.

[0011] The sub-frame 2, the sub-frame 3, the sub-frame 4, the sub-frame 7, the sub-frame 8, and the sub-frame 9 may be the uplink sub-frames;

[0012] the sub-frame 0, the sub-frame 1, the sub-frame 5, and the sub-frame 6 may be the downlink sub-frames; and

[0013] the sub-frame 1 and the sub-frame 6 may be special sub-frames.

[0014] An apparatus for processing baseband uplink and downlink sub-frames, includes at least a serial processing module configured to serially process uplink sub-frames and downlink sub-frames, wherein a length of time slots for processing each sub-frame meets formulae

$$\begin{cases} 3x + 2y + T_{L2} \le 5.0 \text{ ms} \\ 2x + y \le 4 - 2T_a - T_d, \end{cases}$$

[0015] wherein T_a is a delay in transmission from a designated receiving antenna to a baseband processor, T_d is a delay in initiating baseband sub-frame processing, T_{L2} is a time reserved for MAC layer processing, x represents an allowable length of time slots for processing an uplink sub-frame, and y represents an allowable length of time slots for processing a downlink sub-frame.

[0016] An order of processing arrangement in serial processing of the uplink sub-frames and the downlink sub-frames may be: a sub-frame 2 of a current frame, a sub-frame 3 of the current frame, a sub-frame 6 of the current frame, a sub-frame 4 of the current frame, a sub-frame 0 of a next frame, a sub-frame 7 of the current frame, a sub-frame 8 of the current frame, a sub-frame 1 of the next frame, a sub-frame 9 of the current frame, and a sub-frame 5 of the next frame,

[0017] wherein a reserved time slot with a length of at least T_{L2} may be inserted between an uplink sub-frame 4 of the current frame and a downlink sub-frame 0 of the next frame, and the reserved time slot with a length of at least T_{L2} may be inserted between an uplink sub-frame 9 of the current frame and a downlink sub-frame 5 of the next frame.

[0018] According to the above technical solution provided by the present disclosure, the uplink and downlink sub-frames are processed in serial, and the length of the time slots for processing each sub-frame meets the requirement shown in formula (3). Preferably, the order of arranging the processing of the uplink and downlink sub-frames is: sub-frame 2 of the current frame, sub-frame 3 of the current frame, sub-frame 6 (sub-frame S) of the current frame, sub-frame 4 of the current frame, sub-frame 0 of the next frame, sub-frame 7 of the current frame, sub-frame 8 of the current frame, sub-frame 2 (sub-frame S) of the next frame, sub-frame 9 of the current frame and sub-frame 5 of the next frame, wherein a reserved time slot with a length of at least T_{L2} is inserted

between uplink sub-frame 4 (or 9) and downlink sub-frame 0 (or 5) of the next frame. With the method of serial processing of the uplink and downlink sub-frames of the present disclosure, more abundant processing time is obtained. In other words, only a lower speed is required for the baseband processor, thus reducing the idle rate of the baseband processor and improving the resource utilization of the processor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] FIG. **1** is the schematic diagram of the issuance of the uplink and downlink sub-frames of an existing LTE-TDD configuration 0;

[0020] FIG. **2** is the schematic diagram of the uplink and downlink sub-frames and the constraint on a temporal order of the time slots for processing the uplink and downlink sub-frames according to the present disclosure;

[0021] FIG. **3** is the schematic diagram of the order in processing the uplink sub-frames according to the present disclosure; and

[0022] FIG. **4** is the schematic diagram of the order in processing the downlink sub-frames according to the present disclosure.

DETAILED DESCRIPTION

[0023] As the time slots of the uplink and downlink sub-frames of the PUSCH and PDSCH are not completely parallel in time, it is possible to serially process the uplink and downlink with the same processor. With the uplink and downlink serial processing, it is possible to improve the utilization of the processor and decrease an idling rate, thus lowering the cost of implementing a base station system.

[0024] Those skilled in the art know that in seven different configurations of the LTE-TDD, the worst case occurs at configuration 0. FIG. **1** is the schematic diagram of the issuance of the uplink and downlink sub-frames of the existing LTE-TDD configuration 0. In FIG. **1**, blank sub-frames represent the downlink, while shaded sub-frames represent the uplink. Sub-frame S represents a special sub-frame; arrows indicated that information solved from corresponding uplink sub-frames must be sent back to a downlink channel at the downlink sub-frames directed by the arrows. As shown in FIG. **1**, in the case of configuration 0, there are totally six uplink sub-frames and four downlink sub-frames that go through an analysis of arrangement and combination of various different processing time slots under designated parameters such as channel transmission delay T_a, delay in initiating baseband sub-frame processing T_d and time reserved for MAC layer processing T_{L2} and the like.

[0025] FIG. **2** is the schematic diagram of the uplink and downlink sub-frames and the constraint on a temporal order of the time slots for processing the uplink and downlink sub-frames according to the present disclosure. In FIG. **2**, line 1 is the schematic diagram of the issuance of sub-frames of configuration 0, line 2 is the schematic diagram of the time slots for processing the sub-frames by the processor. Parameters such as a delay in transmission from a receiving antenna to a baseband processor T_a, delay in initiating baseband sub-frame processing T_d, time reserved for MAC layer processing T_{L2}, and the like are given in a rhombic frame.

[0026] First, as shown in FIG.2, processing of three uplink sub-frames and two downlink sub-frames, i.e. uplink sub-frame 2 of a current frame, uplink sub-frame 3 of the current frame, uplink sub-frame 4 of the current frame, special downlink sub-frame 6 of the current frame (sub-frame S), downlink sub-frame 0 of a next frame, and an interval T_{L2} must be completed within half of a data frame, i.e. 5 ms, which leads to formula (1):

$$3x+2y+T_{L2}\leq 5.0 \text{ ms} \tag{1}$$

wherein x represents an allowable length of time slots for processing the uplink sub-frame, and y represents an allowable length of time slots for processing the downlink sub-frame.

[0027] Then, it may be known from the special sub-frame S that, as downlink channel transmission delay Ta and the time slots for processing sub-frame S must be completed Ta before the sending of the downlink sub-frame S, formula (2) thus holds:

$$2x+y\leq 4-2T_a-T_d \tag{2}$$

[0028] By combining formula (1) and formula (2), a limiting condition equation of the time slots for uplink and downlink processing is obtained as shown in formula (3):

$$\begin{cases} 3x+2y+T_{L2}\leq 5.0 \text{ ms} \\ 2x+y\leq 4-2T_a-T_d \end{cases} \tag{3}$$

[0029] Analyzing from FIG. **2**, it is clear that, instead of processing sub-frames 0, 1, 2, . . . , 9 according to an existing order therein, the present disclosure processes the sub-frames according to the order of the uplink and downlink sub-frames 2, 3, 6, 4, 0, 7, 8, 1, 9, 5, which is the optimal order. It is easy for those skilled in the art to know that there are a lot of suboptimal orders which will not be enumerated herein. FIG. **3** is the schematic diagram of the order in processing the uplink sub-frames according to the present disclosure. FIG. **4** is the schematic diagram of the order in processing the downlink sub-frames according to the present disclosure. The orders in processing the sub-frames shown in FIG. **3** and FIG. **4** are derived based on the analysis of FIG. **2**. In FIG. **3** and FIG. **4**, the uplink sub-frames are processed according to the order of 2, 3, 4, 7, 8, 9. The special sub-frame 6 (or sub-frame S) is processed between sub-frame 3 and sub-frame 4; the downlink sub-frame 0 of the next data frame is processed between sub-frame 4 and sub-frame 7; the special sub-frame 1 (sub-frame S) of the next data frame is processed between sub-frame 8 and sub-frame 9; and the downlink sub-frame 5 of the next data frame is processed at last. As a signal (if any) solved from the uplink sub-frame 4(or sub-frame 9) must be sent back at the downlink sub-frame 0 (or sub-frame 5), thus a time slot of a length of at least T_{L2}, i.e. reserved time slot, must be inserted between the two sub-frames 4(or 9) and 0 (or 5).

[0030] To sum up, the method for processing baseband uplink and downlink sub-frames according to the present disclosure comprises: serially processing the uplink and downlink sub-frames, wherein the length of the time slots for processing each sub-frame meets the requirement shown in formula (3). Preferably, the order of arranging the processing of the uplink and downlink sub-frames is: a sub-frame 2 of a current frame, a sub-frame 3 of the current frame, a sub-frame 6 of the current frame, a sub-frame 4 of the current frame, a sub-frame 0 of a next frame, a sub-frame 7 of the current frame, a sub-frame 8 of the current frame, a sub-frame 1 of the next frame, a sub-frame 9 of the current frame, and a sub-frame 5 of the next frame, wherein a reserved time slot with a

length of at least T_{L2} is inserted between uplink sub-frame 4 (or 9) of the current frame and downlink sub-frame 0 (or 5) of the next frame.

[0031] Compared with the solution of parallel uplink and downlink processing, the advantages of the method according to the present disclosure are as follows.

[0032] The solution of parallel processing of the uplink and downlink sub-frames must meet:

$$\begin{cases} x \le 1.0 \text{ ms} \\ y \le 1.0 \text{ ms}; \end{cases}$$

[0033] and the solution of serial processing of the uplink and downlink sub-frames must meet:

$$\begin{cases} 3x + 2y + T_{L2} \le 5.0 \text{ ms} \\ 2x + y \le 4 - 2T_a - T_d. \end{cases}$$

[0034] According to the two equations above, it seems that the parallel processing could give more abundant processing time. However, the parallel processing requires parallel operation of two processors, while the serial processing solution only requires one processor. Therefore, it is obvious that the serial processing solution is more advantageous. Specifically speaking:

[0035] assume that the channel transmission delay T_a=0.2 ms, delay in initiating baseband sub-frame processing T_d=1.0 ms, time reserved for MAC layer processing T_{L2}=1.0 ms, and then:

[0036] in the solution of parallel processing of the uplink and downlink sub-frames, let

$$\begin{cases} x = 1.0 \text{ ms} \\ y = 1.0 \text{ ms}; \end{cases}$$

[0037] in the solution of serial processing of the uplink and downlink sub-frames, assume that y=1.0 ms, and then

$$\begin{cases} 3x + 2y + T_{L2} \le 5.0 \text{ ms} \\ 2x + y \le 4 - 2T_a - T_d \end{cases} \Rightarrow \begin{cases} 3x + 2y \le 4.0 \text{ ms} \\ 2x + y \le 2.6 \text{ ms} \end{cases} \Rightarrow \begin{cases} y = 1.0 \text{ ms} \\ x = 0.8 \text{ ms}. \end{cases}$$

[0038] As the solution of serial processing of the uplink and downlink sub-frames only requires one processor, while the parallel processing solution requires two processors, the solution of serial processing of the uplink and downlink sub-frames according to the present disclosure is more advantageous and obtains more abundant processing time. In other words, only a lower speed is required for the baseband processor, thus reducing the idle rate of the baseband processor and improving the resource utilization of the processor.

[0039] With respect to the method according to the present disclosure, an apparatus for processing baseband uplink and downlink sub-frames is further provided. The apparatus according to the present disclosure may be set at the base station side and includes at least a serial processing module configured to serially process uplink and downlink sub-frames, wherein a length of time slots for processing each sub-frame meets the requirement of formula (3). The serial processing module is further configured to perform serial processing according to the following order in processing the uplink and downlink sub-frames: a sub-frame 2 of a current frame, a sub-frame 3 of the current frame, a sub-frame 6 of the current frame, a sub-frame 4 of the current frame, a sub-frame 0 of a next frame, a sub-frame 7 of the current frame, a sub-frame 8 of the current frame, a sub-frame 1 of the next frame, a sub-frame 9 of the current frame, and a sub-frame 5 of the next frame, wherein a reserved time slot with a length of at least T_{L2} is inserted between uplink sub-frame 4 (or 9) of the current frame and downlink sub-frame 0 (or 5) of the next frame.

[0040] What described are merely preferred embodiments of the present disclosure and are not intended to limit the scope of the present disclosure. Any modifications, equivalent replacements and improvements within the spirit and principle of the present disclosure should be contained in the protection scope of the present disclosure.

1. A method for processing baseband uplink and downlink sub-frames, comprising:

serially processing uplink sub-frames and downlink sub-frames at a base station side of a Long Term Evolution-Time Division Duplex (LTE-TDD) system, wherein a length of time slots for processing each sub-frame meets formulae

$$\begin{cases} 3x + 2y + T_{L2} \le 5.0 \text{ ms} \\ 2x + y \le 4 - 2T_a - T_d, \end{cases}$$

wherein T_a is a delay in transmission from a designated receiving antenna to a baseband processor, T_d is a delay in initiating baseband sub-frame processing, T_{L2} is a time reserved for MAC layer processing, x represents an allowable length of time slots for processing an uplink sub-frame, and y represents an allowable length of time slots for processing a downlink sub-frame.

2. The method for processing baseband uplink and downlink sub-frames according to claim **1**, wherein an order of processing arrangement in the serially processing uplink sub-frames and downlink sub-frames is: a sub-frame 2 of a current frame, a sub-frame 3 of the current frame, a sub-frame 6 of the current frame, a sub-frame 4 of the current frame, a sub-frame 0 of a next frame, a sub-frame 7 of the current frame, a sub-frame 8 of the current frame, a sub-frame 1 of the next frame, a sub-frame 9 of the current frame, and a sub-frame 5 of the next frame, wherein a reserved time slot with a length of at least T_{L2} is inserted between the sub-frame 4 of the current frame and the sub-frame 0 of the next frame, and the reserved time slot with a length of at least T_{L2} is inserted between the sub-frame 9 of the current frame and the sub-frame 5 of the next frame.

3. The method for processing baseband uplink and downlink sub-frames according to claim **2**, wherein the sub-frame 2, the sub-frame 3, the sub-frame 4, the sub-frame 7, the sub-frame 8, and the sub-frame 9 are the uplink sub-frames;

the sub-frame 0, the sub-frame 1, the sub-frame 5, and the sub-frame 6 are the downlink sub-frames; and

the sub-frame 1 and the sub-frame 6 are special sub-frames.

4. An apparatus for processing baseband uplink and downlink sub-frames, comprising at least a serial processing mod-

ule configured to serially process uplink sub-frames and downlink sub-frames, wherein a length of time slots for processing each sub-frame meets formulae

$$\begin{cases} 3x + 2y + T_{L2} \le 5.0 \text{ ms} \\ 2x + y \le 4 - 2T_a - T_d, \end{cases}$$

wherein T_a is a delay in transmission from a designated receiving antenna to a baseband processor, T_d is a delay in initiating baseband sub-frame processing, T_{L2} is a time reserved for MAC layer processing, x represents an allowable length of time slots for processing an uplink sub-frame, and y represents an allowable length of time slots for processing a downlink sub-frame.

5. The apparatus for processing baseband uplink and downlink sub-frames according to claim **4**, wherein an order of processing arrangement in serial processing of the uplink sub-frames and the downlink sub-frames is: a sub-frame 2 of a current frame, a sub-frame 3 of the current frame, a sub-frame 6 of the current frame, a sub-frame 4 of the current frame, a sub-frame 0 of a next frame, a sub-frame 7 of the current frame, a sub-frame 8 of the current frame, a sub-frame 1 of the next frame, a sub-frame 9 of the current frame, and a sub-frame 5 of the next frame,

wherein a reserved time slot with a length of at least T_{L2} is inserted between an uplink sub-frame 4 of the current frame and a downlink sub-frame 0 of the next frame, and the reserved time slot with a length of at least T_{L2} is inserted between an uplink sub-frame 9 of the current frame and a downlink sub-frame 5 of the next frame.

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