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(54) **HIGH PRECISION ALGORITHMICALLY ASSISTED VOLTAGE DIVIDER WITH FAULT DETECTION**

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(57) **ABSTRACT**

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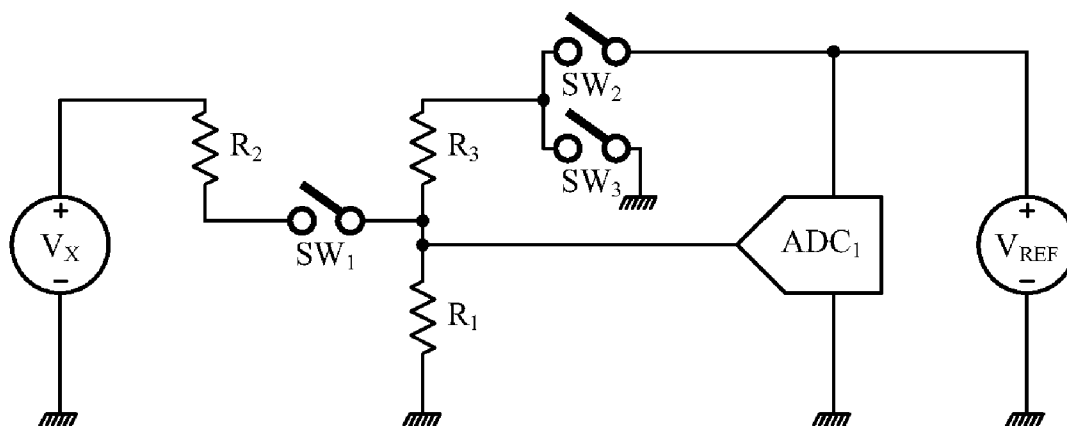
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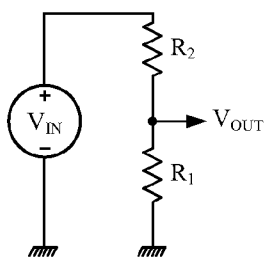
**Related U.S. Application Data**

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A method, an algorithm, and circuits for implementation of a high-accuracy voltage divider are described that include a capability of fault detection. The disclosure allows for correction of non-catastrophic faults, such as significant changes of the components' values. The performance of the circuit built as described is vastly superior to operations achievable with the modern-day components utilized in previous standard and known configurations.



Exemplary circuit for current invention



$$V_{OUT} = \frac{R_1}{R_1 + R_2} \cdot V_{IN}$$

Figure 1 Prior art

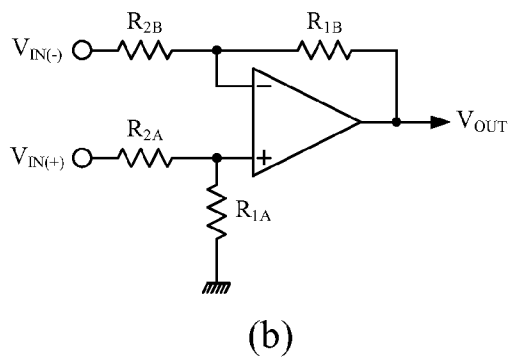
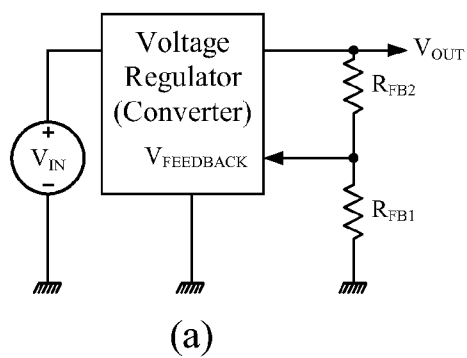


Figure 2 Prior art

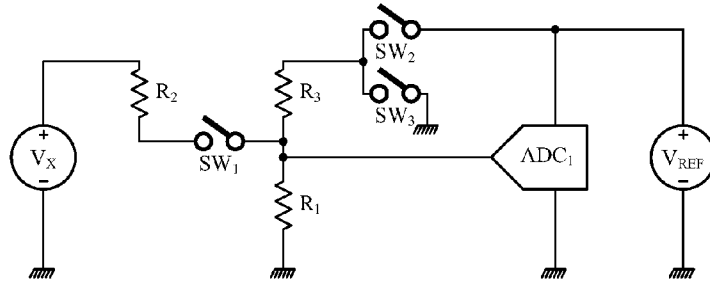


Figure 3 Exemplary circuit for current invention

Step #	SW <sub>1</sub>	SW <sub>2</sub>	SW <sub>3</sub>	ADC <sub>1</sub> V <sub>in</sub>
1	Open	<b>Closed</b>	Open	$V_1 = \frac{R_1}{R_1 + R_3} \cdot V_{REF}$
2	<b>Closed</b>	Open	Open	$V_2 = \frac{R_1}{R_1 + R_2} \cdot V_X$
3	<b>Closed</b>	Open	<b>Closed</b>	$V_3 = \frac{R_{1\parallel 3}}{R_{1\parallel 3} - R_2} \cdot V_X$
4	<b>Closed</b>	<b>Closed</b>	Open	$V_4 = \frac{R_{1\parallel 3}}{R_{1\parallel 3} + R_2} \cdot V_X + \frac{R_{1\parallel 2}}{R_{1\parallel 2} + R_3} \cdot V_{REF}$
$R_{1\parallel 3} = \frac{R_1 \cdot R_3}{R_1 + R_3}$ (for Steps 3 and 4); $R_{1\parallel 2} = \frac{R_1 \cdot R_2}{R_1 + R_2}$ (for Step 4)				

(a)

(b) 
$$V_X = V_2 \cdot \left\{ 1 + \frac{\left(1 - \frac{V_1}{V_{REF}}\right) \cdot (V_4 - V_3)}{(V_1 + V_3 - V_4)} \right\}$$

(c) 
$$V_X - V_2 \cdot \left\{ 1 + \frac{V_4 - V_3}{2 \cdot (V_1 + V_3 - V_4)} \right\} \quad (\text{when } R_1 = R_3)$$

Figure 4 Method and algorithm (a), formula for calculation of V<sub>X</sub> (b), and simplified formula (c).

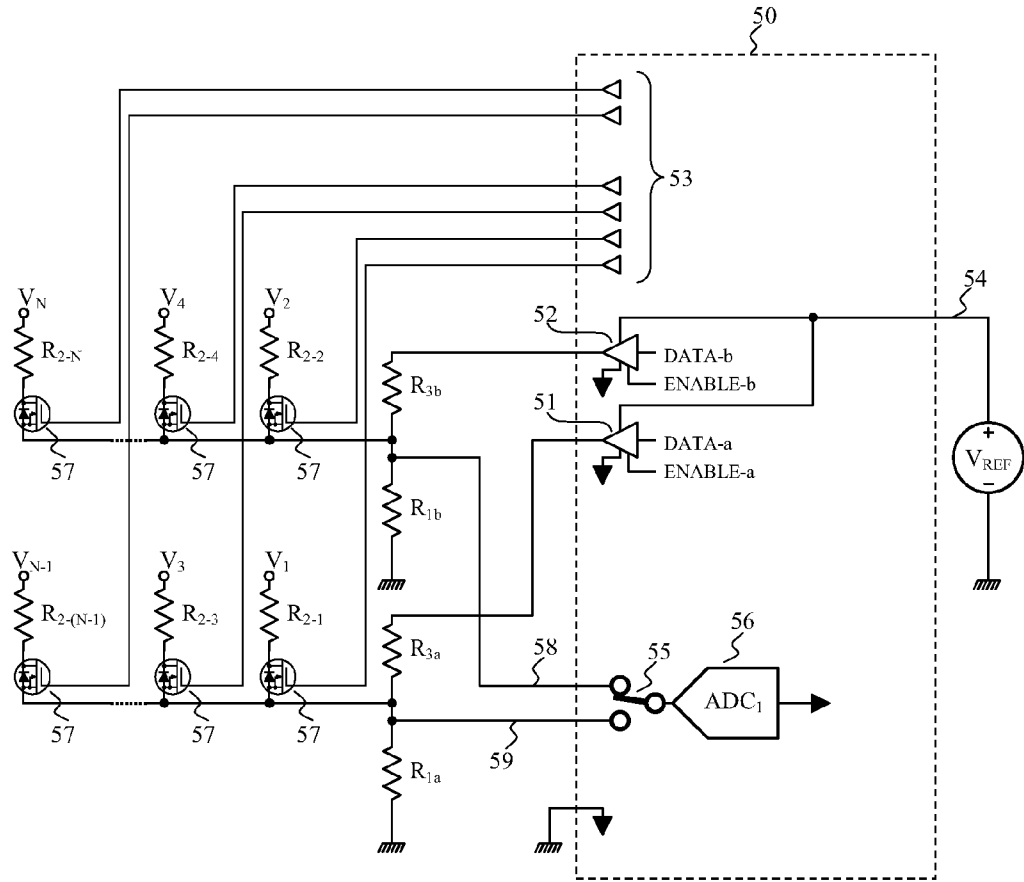


Figure 5 Multiple-input Instrumentation Amplifier according to current invention

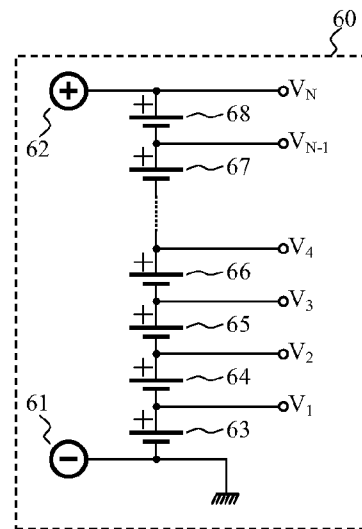


Figure 6 Battery made up from series-connected cells

## HIGH PRECISION ALGORITHMICALLY ASSISTED VOLTAGE DIVIDER WITH FAULT DETECTION

### BACKGROUND

[0001] One of the commonly utilized circuits in any electronic device is a voltage divider shown in FIG. 1. An input voltage  $V_{IN}$  can be scaled according to the ratio of resistors  $R_1$  and  $R_2$ ; one is able to calculate the output voltage of the divider by well-known formula in FIG. 1.

[0002] Two familiar applications for the voltage divider are depicted in FIG. 2.

[0003] Shown in (a) is the typical circuit for the voltage regulator; the voltage divider consisting of  $R_{FB1}$  and  $R_{FB2}$  generates a feedback voltage  $V_{FEEDBACK}$  that is used to regulate the output voltage  $V_{OUT}$ . The alert reader will immediately recognize that any faults within the voltage divider will produce an abnormal output voltage from the regulator; this may lead to destruction of the whole device that incorporates this voltage regulator, as well as to smoke and fire.

[0004] For example, if resistor  $R_{FB2}$  is opened (due to overheating, failure of the solder, or any other reason), the voltage regulator circuit will assume that the output is low, near 0 V, and will try to increase it uncontrollably.

[0005] Therefore, it is typical that any circuit that may produce dangerous output in case of the divider fault includes some redundancy or an independent control mechanism to limit the maximum output. A characteristic solution for the voltage regulator is to utilize two voltage dividers, with the circuit inside of the voltage regulator being able to select the highest feedback voltage, and thus limit the output; alternatively, a separate over-voltage protection circuit is employed.

[0006] Illustrated in FIG. 2 (b) is a so-called Instrumentation Amplifier (IA), a circuit that is able to produce at the output an amplified difference between the two input signals.

[0007] An important characteristic of the IA is the Common Mode Rejection Ratio (CMRR), an ability to reject changes in input voltages that are common to both inputs, while the difference between the inputs gets amplified and goes through unimpeded.

[0008] With the common-day state-of-the-art components it is possible to create an IA circuit of this configuration that boasts a CMRR value of, perhaps, 20-48 dB (utilizing the 0.1% accurate resistors, that are the best available for practical use). Any further improvement of CMRR is achieved by manually trimming the value of one or several resistors.

[0009] However, even a perfectly adjusted IA will tend to lose the CMRR value when operated over some temperature range, and specifically when operated at a temperature other than at the temperature at which the adjustments were made. This is due to resistors having various temperatures and/or various temperature coefficients. It will be appreciated that the best possible practical performance for this type of the circuit is on the order of 1% or worse. It is only with strict laboratory conditions and very expensive high-accuracy resistors that better performance is achievable.

[0010] On the other hand, the IA constructed according to FIG. 2 (b) is able safely to sense voltages that are many times higher than the supply voltage of the Operational Amplifier, which is a very desirable property.

[0011] In a typical system, it is likely that an Analog-to-digital converter will follow the IA, and the IA output will thus be converted to a digital value. Also it is likely that in a

modern-day system a microcontroller will make sense of and act upon the values received from the IA.

[0012] Furthermore, present-day analog-to-digital converters can have an accuracy and resolution that is many times better than the best-possible performance available from the IA circuit in FIG. 2 (b).

### DESCRIPTIONS OF THE DRAWINGS

[0013] This invention will be described with respect to several drawings, of which:

[0014] FIGS. 1 and 2 depict prior-art circuits,

[0015] FIG. 3 presents an exemplary circuit making use of the invention;

[0016] FIG. 4 describes a method and algorithm, and shows formulas for calculations;

[0017] FIG. 5 demonstrates a multiple-input Instrumentation Amplifier created according to the invention; and

[0018] FIG. 6 illustrates a battery created with series-connected cells; the circuit in FIG. 5 is superbly suitable for measurements of all the voltages in such a battery.

### DETAILED DESCRIPTION

[0019] The current invention teaches a method, an algorithm, and circuits for implementation of a high-accuracy voltage divider that includes a capability of fault detection.

[0020] Presented in FIG. 3 is the exemplary circuit for the current invention. In addition to  $R_1$  and  $R_2$  that were part of the original circuit for the voltage divider of FIG. 1, there are several components (resistors and switches) that make possible the new properties of high accuracy and fault detection.

[0021] Also present is the Analog-to-digital converter that is typically a part of any contemporary electronic device; the closing and opening of the switches would most likely be governed by a microcontroller that is also a typical part of modern-day devices.

[0022] If several measurements are performed according to an algorithm described in FIG. 4(a), an unknown voltage  $V_x$  can be calculated from the formula presented in FIG. 4(b). As will be appreciated, the calculated value of the unknown voltage  $V_x$  is independent of the values of the resistors.

[0023] In other words, if one or all resistors changed their values (due to temperature, ageing, mechanical stress, or any other effects), the calculated value of the unknown voltage  $V_x$  would still be accurate.

[0024] Using similar formulas (not shown for clarity, but readily derivable by the alert reader), the individual values for all resistors and/or ratios between the resistors can be calculated; deviations in excess of preset limits will be promptly recognized by a microcontroller, and can be reported as a detected fault.

[0025] In addition, such deviations will prompt the microcontroller to behave in a specific way that will place the system in a known and safe state. Such behavior may include (but is not limited to) shutting down the supply voltages, disconnecting the loads, and preventing the human operator from using a faulty device.

[0026] A special case that allows for simplification of the formula is shown in FIG. 4(c); a necessary condition for this simplification is that  $R_1=R_3$ . However, the system may still periodically check that condition  $R_1=R_3$  is in fact precise to the desired accuracy.

[0027] Describing individual steps within the algorithm of FIG. 4 (a):

[0028] In Step #1 switch SW<sub>2</sub> is closed and measurement V<sub>1</sub> is obtained (as a digitally coded result from ADC<sub>1</sub>); the expected value is shown under heading "ADC<sub>1</sub> V<sub>in</sub>" in the table FIG. 4(a).

[0029] In Step #2 switch SW<sub>1</sub> is closed and measurement V<sub>2</sub> is obtained.

[0030] In Step #3 switches SW<sub>1</sub> and SW<sub>3</sub> are closed and measurement V<sub>3</sub> is obtained.

[0031] And finally, in Step #4 switches SW<sub>1</sub> and SW<sub>2</sub> are closed and measurement V<sub>4</sub> is obtained.

[0032] Substituting the above measured values into formula FIG. 4 (b) or (c), one can find the unknown value V<sub>x</sub>.

[0033] The exact order of the above four (4) steps is not important, they may in fact be executed in whatever sequence is conducive to and coherent with other system processes.

[0034] The accuracy of the calculated voltage V<sub>x</sub> depends only on the accuracy of the Analog-to-digital converter. As described above, the typical A/D unit in a modern device is routinely many times more accurate than the accuracy of an unaided resistive voltage divider.

[0035] Described in FIG. 5 is a multiple-input (e.g. multiplexed) Instrumentation Amplifier that utilizes voltage dividers according to the invention.

[0036] An alert reader will recognize that the circuit in FIG. 5 includes two independent voltage divider channels, each similar to the depiction in FIG. 3.

[0037] A microcontroller 50 has internal circuits 51, 52, 55, and 56.

[0038] Circuits 51 and 52 are ports typically used for digital input/output, but utilized here instead of switches SW<sub>2</sub> and SW<sub>3</sub> of FIG. 3, with exactly the same functionality.

[0039] Circuit 56, with the aid of circuit 55, corresponds to an Analog-to-digital converter with multiplexed input; alternatively, and with better performance, a microcontroller with dual on-board A/D converters can be used.

[0040] Alternatively, circuit 55 could be eliminated and nodes 58 and 59 combined, thus permitting the elimination of some other system elements such as driver 52 and resistors R<sub>3b</sub> and R<sub>1b</sub>.

[0041] Digital drivers 53 control the voltage on the gates of n-channel MOSFET switches 57; only one MOSFET switch connected to R<sub>1a</sub>/R<sub>3a</sub> and one MOSFET switch connected to R<sub>1b</sub>/R<sub>3b</sub> should be activated (turned On) at the same time.

[0042] It will be appreciated that the gate voltage on the MOSFET switch should be sufficiently large in relation to the voltage on lines 58 and 59, in order to fully enhance (turn On) the corresponding switch.

[0043] When the MOSFET switch is fully turned On, it still has some residual resistance; however, the action of the algorithm will accommodate this additional resistance, as it will simply manifest itself as slight increase of corresponding resistors R<sub>2-n</sub>; as described above, the algorithm is not sensitive to the actual value of all resistors.

[0044] It will likewise be appreciated that there are obvious limitations, namely, the normal operating input range of the A/D converter 56 should not be violated as the result of the resistance changes.

[0045] The configuration of FIG. 5 is suited for measurements of voltages that are positive in respect to ground; obvious steps can be taken in order to make this circuit operational with negative voltages as well as with voltages that are both positive and negative in respect to ground; such steps may

include utilization of p-channel MOSFETs, or pairs of n-channel or p-channel MOSFETs in order to make all switches bi-directional-blocking

[0046] After the two unknown voltages are calculated (one in each channel of measurements), the difference between the two voltages is obtained digitally, inside microcontroller 50. Then, the difference voltage can be used in the same manner as if it had been obtained from an actual old-configuration IA of FIG. 2(b).

[0047] FIG. 6 shows one system that is well suited for measurements with the circuit in FIG. 5. A battery 60 is created by serially connecting cells 63 through 68. As a part of the control system for such a battery, it will be necessary to measure voltages V<sub>1</sub> through V<sub>N</sub>. A circuit such as in FIG. 5 is ideally suited for the job.

[0048] It is noted that the examples given above refer to a "ground" and to a V<sub>REF</sub> that is positive relative to ground. Such designations are, of course, completely arbitrary and are employed merely for economy of description. Every circuit portrayed here could be just as well set up with opposite sense, for example with V<sub>REF</sub> being negative relative to ground.

[0049] The alert reader, having learned the teachings given herein, will have no difficulty devising myriad obvious improvements and variants of the invention, all of which are intended to be encompassed within the scope of the claims below.

1. Apparatus for measuring a voltage at a terminal, the apparatus comprising:

- an A/D converter having an analog input and a digital output, the A/D converter measuring its input relative to a VREF and to a ground;
- a first resistance connected between the analog input of the A/D converter and the ground;
- a first switch controllably connecting the analog input of the A/D converter through a second resistance to the terminal;
- a third resistance connected between the analog input of the A/D converter and a first node;
- a second switch controllably connecting the first node to the VREF;
- a third switch controllably connecting the first node to the ground.

2. The apparatus of claim 1 in which the first resistance is substantially equal in resistance to the third resistance.

3. The apparatus of claim 1 further comprising a control means, the control means disposed to carry out the steps of:

- closing the second switch at a time when the first switch and the third switch are open, and measuring a first voltage at the analog input of the A/D converter;
- closing the first switch at a time when the second switch and the third switch are open, and measuring a second voltage at the analog input of the A/D converter;
- closing the first switch and the third switch at a time when the second switch is open, and measuring a third voltage at the analog input of the A/D converter; and
- closing the first switch and the second switch at a time when the third switch is open, and measuring a first voltage at the analog input of the A/D converter.

4. The apparatus of claim 3 wherein the control means is further characterized in that the first, second, third, and fourth closings take place in the sequence set forth.

5. A method for use with apparatus comprising an A/D converter having an analog input and a digital output, the A/D

converter measuring its input relative to a VREF and to a ground, the apparatus further comprising a first resistance, a second resistance, and a third resistance, the first resistance connected between the analog input of the A/D converter and the ground, the method carried out with respect to a terminal, the method comprising the steps of:

- connecting the third resistance between the analog input of the A/D converter and the VREF, and measuring a first voltage at the analog input of the A/D converter;
- connecting the second resistance between the terminal and the analog input of the A/D converter, and measuring a second voltage at the analog input of the A/D converter;
- connecting the second resistance between the terminal and the analog input of the A/D converter and connecting the third resistance between the analog input of the A/D converter and the ground, and measuring a third voltage at the analog input of the A/D converter; and
- connecting the second resistance between the terminal and the analog input of the A/D converter and connecting the third resistance between the analog input of the A/D converter and the VREF, and measuring a fourth voltage at the analog input of the A/D converter.

6. The method of claim 5 in which the first resistance is substantially equal in resistance to the third resistance.

7. The method of claim 5 wherein the first, second, third, and fourth closing steps take place in the sequence set forth.

8. The method of claim 5 further comprising the step, performed after the first, second, third, and fourth closing steps, of evaluating a function of the first, second, third, and fourth voltages to yield a measured voltage at the terminal.

9. The method of claim 5 wherein the measuring of voltage at the analog input of the A/D converter further comprises observing the voltage at several distinct times so as to evaluate whether the voltage is settled.

10. The method of claim 5 further comprising the step, performed after the first, second, third, and fourth closing steps, of evaluating a function of the first, second, third, and fourth voltages to yield a measured value for the first resistance, the second resistance, and the third resistance.

11. The method of claim 10 further comprising the step of comparing measured values for the first resistance, the second resistance, and the third resistance at various times, whereby any large change in the first resistance or the second resistance or the third resistance may be detected.

12. Apparatus for measuring a voltage at each of a plurality of terminals, the apparatus comprising:

- a A/D converter having an analog input and a digital output, the A/D converter measuring its input relative to a VREF and to a ground;
- a first resistance connected between the analog input of the A/D converter and the ground;
- a plurality of first switches, each one of the first switches associated with a respective one of the plurality of terminals;
- a plurality of second resistances, each one of the second resistances associated with a respective one of the plurality of terminals;
- each one of the first switches controllably connecting the analog input of the A/D converter to its respective terminal through the terminal's respective second resistance;
- a third resistance connected between the analog input of the A/D converter and a first node;

- a second switch controllably connecting the first node to the VREF;
- a third switch controllably connecting the first node to the ground.

13. The apparatus of claim 12 in which the first resistance is substantially equal in resistance to the third resistance.

- 14. The apparatus of claim 12 further comprising a control means, the control means disposed to carry out the steps of:
  - closing the second switch at a time when the first switches and the third switch are open, and measuring a first voltage at the analog input of the A/D converter;
  - closing one of the first switches at a time when the second switch and the third switch are open, and measuring a second voltage at the analog input of the A/D converter;
  - closing the same one of the first switches and the third switch at a time when the second switch is open, and measuring a third voltage at the analog input of the A/D converter; and
  - closing the same one of the first switches and the second switch at a time when the third switch is open, and measuring a first voltage at the analog input of the A/D converter.

15. The apparatus of claim 14 wherein the control means is further characterized in that the first, second, third, and fourth closings take place in the sequence set forth.

16. A method for use with respect to a plurality of terminals, the method for use with respect to apparatus comprising an A/D converter having an analog input and a digital output, the A/D converter measuring its input relative to a VREF and to a ground, the apparatus further comprising a first resistance, a plurality of second resistances, each of the second resistances associated with a respective one of the terminals, and a third resistance, the first resistance connected between the analog input of the A/D converter and the ground, the method comprising the steps of:

- connecting the third resistance between the analog input of the A/D converter and the VREF, and measuring a first voltage at the analog input of the A/D converter;
- connecting one of the second resistances between its respective terminal and the analog input of the A/D converter, and measuring a second voltage at the analog input of the A/D converter;
- connecting the same one of the second resistances between its respective terminal and the analog input of the A/D converter and connecting the third resistance between the analog input of the A/D converter and the ground, and measuring a third voltage at the analog input of the A/D converter; and
- connecting the same one of the second resistances between its respective terminal and the analog input of the A/D converter and connecting the third resistance between the analog input of the A/D converter and the VREF, and measuring a fourth voltage at the analog input of the A/D converter.

17. The method of claim 16 in which the first resistance is substantially equal in resistance to the third resistance.

18. The method of claim 16 wherein the first, second, third, and fourth connecting steps take place in the sequence set forth.

19. The method of claim 16 further comprising the step, performed after the first, second, third, and fourth connecting steps, of evaluating a function of the first, second, third, and fourth voltages to yield a measured voltage at the respective terminal.

**20.** The method of claim **16** wherein the measuring of voltage at the analog input of the A/D converter further comprises observing the voltage at several distinct times so as to evaluate whether the voltage is settled.

**21.** The method of claim **16** further comprising the step, performed after the first, second, third, and fourth connecting steps, of evaluating a function of the first, second, third, and fourth voltages to yield a measured value for the first resistance, the one of the second resistances, and the third resistance.

**22.** The method of claim **21** further comprising the step of comparing measured values for the first resistance, the one of the second resistances, and the third resistance at various times, whereby any large change in the first resistance or the one of the second resistances or the third resistance may be detected.

**23.** Apparatus for measuring a voltage at each of a first plurality of terminals and at each of a second plurality of terminals, the apparatus comprising:

- a first A/D converter having an analog input and a digital output, the A/D converter measuring its input relative to a VREF and to a ground;
- a second A/D converter having an analog input and a digital output, the A/D converter measuring its input relative to the VREF and to the ground;
- a first resistance connected between the analog input of the first A/D converter and the ground;
- a fourth resistance connected between the analog input of the second A/D converter and the ground;
- a plurality of first switches, each one of the first switches associated with a respective one of the first plurality of terminals;
- a plurality of fourth switches, each one of the fourth switches associated with a respective one of the second plurality of terminals;
- a plurality of second resistances, each one of the second resistances associated with a respective one of the first plurality of terminals;
- a plurality of fifth resistances, each one of the fifth resistances associated with a respective one of the second plurality of terminals;
- each one of the first switches controllably connecting the analog input of the first A/D converter to its respective terminal through the terminal's respective second resistance;
- each one of the fourth switches controllably connecting the analog input of the second A/D converter to its respective terminal through the terminal's respective fifth resistance;
- a third resistance connected between the analog input of the first A/D converter and a first node;
- a sixth resistance connected between the analog input of the second A/D converter and a second node;
- a second switch controllably connecting the first node to the VREF;
- a fifth switch controllably connecting the second node to the VREF;
- a third switch controllably connecting the first node to the ground.
- a sixth switch controllably connecting the second node to the ground.

**24.** The apparatus of claim **23** in which the first resistance is substantially equal in resistance to the third resistance and the fourth resistance is substantially equal in resistance to the sixth resistance.

**25.** The apparatus of claim **23** further comprising a control means, the control means disposed to carry out the steps of:

- closing the second switch at a time when the first switches and the third switch are open, and measuring a first voltage at the analog input of the first A/D converter;
- closing one of the first switches at a time when the second switch and the third switch are open, and measuring a second voltage at the analog input of the first A/D converter;
- closing the same one of the first switches and the third switch at a time when the second switch is open, and measuring a third voltage at the analog input of the first A/D converter;
- closing the same one of the first switches and the second switch at a time when the third switch is open, and measuring a first voltage at the analog input of the first A/D converter;
- closing the fifth switch at a time when the fourth switches and the sixth switch are open, and measuring a fifth voltage at the analog input of the second A/D converter;
- closing one of the fourth switches at a time when the fifth switch and the sixth switch are open, and measuring a sixth voltage at the analog input of the second A/D converter;
- closing the same one of the fourth switches and the sixth switch at a time when the fifth switch is open, and measuring a seventh voltage at the analog input of the second A/D converter; and
- closing the same one of the fourth switches and the fifth switch at a time when the sixth switch is open, and measuring an eighth voltage at the analog input of the second A/D converter.

**26.** The apparatus of claim **25** wherein the control means is further characterized in that the first, second, third, and fourth closings take place in the sequence set forth and the fifth, sixth, seventh, and eighth closings take place in the sequence set forth.

**27.** A method for use with respect to a first plurality of terminals and a second plurality of terminals, the method for use with respect to apparatus comprising a first A/D converter having an analog input and a digital output, the first A/D converter measuring its input relative to a VREF and to a ground, the apparatus further comprising a second A/D converter having an analog input and a digital output, the second A/D converter measuring its input relative to the VREF and to the ground, the apparatus further comprising a first resistance, a plurality of second resistances, each of the second resistances associated with a respective one of the first plurality of terminals, and a third resistance, the first resistance connected between the analog input of the first A/D converter and the ground, the apparatus further comprising a fourth resistance, a plurality of fifth resistances, each of the fifth resistances associated with a respective one of the second plurality of terminals, and a sixth resistance, the fourth resistance connected between the analog input of the second A/D converter and the ground, the method comprising the steps of:

- connecting the third resistance between the analog input of the first A/D converter and the VREF, and measuring a first voltage at the analog input of the first A/D converter;



connecting one of the second resistances between the terminal and the analog input of the first A/D converter, and measuring a second voltage at the analog input of the first A/D converter;

connecting the same one of the second resistances between its respective terminal and the analog input of the first A/D converter and connecting the third resistance between the analog input of the first A/D converter and the ground, and measuring a third voltage at the analog input of the first A/D converter;

connecting the same one of the second resistances between its respective terminal and the analog input of the first A/D converter and connecting the third resistance between the analog input of the first A/D converter and the VREF, and measuring a fourth voltage at the analog input of the A/D converter;

connecting the sixth resistance between the analog input of the second A/D converter and the VREF, and measuring a fifth voltage at the analog input of the second A/D converter;

connecting one of the fifth resistances between its respective terminal and the analog input of the second A/D converter, and measuring a sixth voltage at the analog input of the second A/D converter;

connecting the same one of the second resistances between its respective terminal and the analog input of the second A/D converter and connecting the sixth resistance between the analog input of the second A/D converter and the ground, and measuring a seventh voltage at the analog input of the second A/D converter; and

connecting the same one of the second resistances between its respective terminal and the analog input of the second A/D converter and connecting the sixth resistance between the analog input of the second A/D converter and the VREF, and measuring an eighth voltage at the analog input of the second A/D converter.

**28.** The method of claim 27 in which the first resistance is substantially equal in resistance to the third resistance and the fourth resistance is substantially equal in resistance to the sixth resistance.

**29.** The method of claim 27 wherein the first, second, third, and fourth connecting steps take place in the sequence set

forth, and wherein the fifth, sixth, seventh, and eighth connecting steps take place in the sequence set forth.

**30.** The method of claim 27 further comprising the step, performed after the first, second, third, and fourth connecting steps, of evaluating a function of the first, second, third, and fourth voltages to yield a measured voltage at the respective terminal to the one of the second resistances, and further comprising the step, performed after the fifth, sixth, seventh and eighth connecting steps, of evaluating a function of the fifth, sixth, seventh, and eighth voltages to yield a measured voltage at the respective terminal to the one of the fifth resistances.

**31.** The method of claim 27 wherein the measuring of voltage at the analog input of the first A/D converter further comprises observing the voltage at several distinct times so as to evaluate whether the voltage is settled, and wherein the measuring of voltage at the analog input of the second A/D converter further comprises observing the voltage at several distinct times so as to evaluate whether the voltage is settled.

**32.** The method of claim 51 further comprising the step, performed after the first, second, third, and fourth connecting steps, of evaluating a function of the first, second, third, and fourth voltages to yield a measured value for the first resistance, the one of the second resistances, and the third resistance, and further comprising the step, performed after the fifth, sixth, seventh and eighth connecting steps, of evaluating a function of the fifth, sixth, seventh and eighth voltages to yield a measured value for the fourth resistance, the one of the fifth resistances, and the sixth resistance.

**33.** The method of claim 32 further comprising the step of comparing measured values for the first resistance, the one of the second resistances, and the third resistance at various times, whereby any large change in the first resistance or the one of the second resistances or the third resistance may be detected, and further comprising the step of comparing measured values for the fourth resistance, the one of the fifth resistances, and the sixth resistance at various times, whereby any large change in the fourth resistance or the one of the fifth resistances or the sixth resistance may be detected.

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