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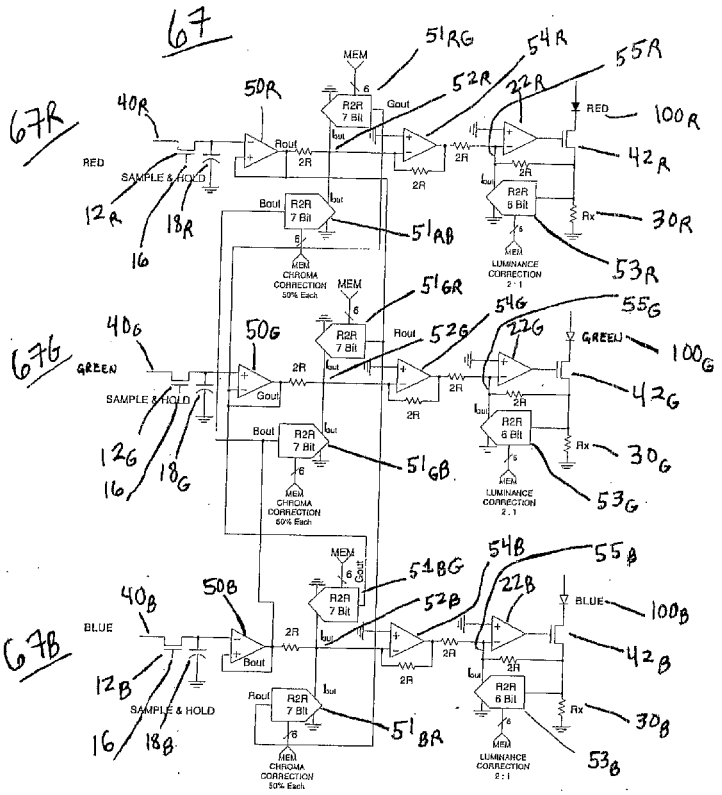

(57) Abstract: A system is used with pixels, each pixel having at least three light-emitting diodes of at least three distinct colors. A driver chip is used which has, for each diode in the pixel, a sample-and-hold circuit which samples an analog video signal for the diode. A luminance-correction circuit draws upon a stored digital luminance correction factor and applies a luminance correction to the driver, the luminance correction factor being stored contiguous to the pixels. A chrominance-correction circuit draws upon stored digital chrominance correction factors for a diode in the pixel and upon signals indicative of the held signals for the other diodes in the pixel, and applies a chrominance correction to the driver input. The chrominance correction factors are also stored contiguous to the pixels.

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LED DRIVER APPARATUS AND METHOD

BACKGROUND

The invention relates generally to large video display systems using light-emitting diodes (LEDs), and relates more particularly to methods and apparatus for driving the LEDs.

Experience shows that it is not easy to drive LEDs of large video displays. Some prior-art approaches are very hardware-intensive, requiring substantial processing power and large numbers of integrated circuits. Many, if not most, prior-art approaches fail to address the problem that LEDs vary in brightness (as a function of drive current) and are non-uniform in dominant wavelength (color). LEDs also vary in forward voltage drop.

The present practice is to assemble LEDs into an array of some convenient size using red, green and blue LEDs that have a reasonable intensity match, and drive the LEDs with a constant-current driver to compensate for variations in forward voltages in the LEDs of the same color. This array of LEDs are driven at the current level of intended use, and then measured and their color coordinates as detailed on the C.I.E. 1931 Chromaticy Diagram and stored in a convenient memory. A correction value for each PEL of each pixel is then calculated, one value for each of the two companion PELs that will be modified to correct the display PEL, for a total of six correction values for each pixel. These correction values are then stored in a correction memory frame where each pixel on the final display has a correction memory site for the six correction values.

The image to be displayed is also stored in a display frame memory where each pixel on the final display has a display memory site to store the digital value for the pixel to be displayed. The number of bits in the display memory are typically from 8 bits to 12 bits in length, but may greater. The display value is then multiplied by each of the six correction values to derive the final value for display. This value may be displayed in a corrected memory, or parsed out in

multiple refresh memories as the system requires.

If the image is stored in a typical computer, then the pixel rate may be in the order of 25 million pixels per second, requiring 150 million multiplication operations of 8- to 12-bit display numbers by 6- to 10-bit correction numbers per second. This is a formidable task, and is usually accomplished by using multiple processors.

As mentioned above, in some present-day systems, to compensate for variations in forward voltage drop, the LED drivers use a constant-current drive. With many such drivers, the current is set by operating voltages or with current regulators. The intensity the LED is generally controlled by pulse-width modulation. The overall intensity of the display may be varied by either selecting alternate pulse-width time periods, or by deleting small time segments of the LEDs that have been activated.

Many displays used for video systems use eight bits to define the intensity for each of the red, blue and green LEDs. Eight bits yield 256 intensity levels for each of the three colors for a total of 16,777,216 color combinations.

To accomplish video display in a pulse-width modulated system requires that the screen face be refreshed eight times with variable display intervals for each field within the frame time of standard video of 30 frames per second. A phosphor-based display benefits from time averaging due to the non-instantaneous decay rate of the phosphors, and as a consequence, 30 frames per second is adequate for phosphor based video displays. LEDs, however, turn on essentially instantly and turn off essentially instantly. If a refresh rate of only 30 frames per second is used (with pulse-width-modulated drive), this is not adequate for LED displays, because such a refresh rate gives rise to viewing artifacts are perceived by human observers. To remove or eliminate such viewing artifacts, it is typically necessary to refresh the display at 120 frames per second. This is a very difficult task for video-based display systems of 320 by 256 pixels or larger and requires multiple processors to accomplish the task. Stated differently, such drivers require

substantial processing and communications bandwidth to refresh the display frequently enough to provide a smooth display that is free from perceptible artifacts.

Prior efforts to solve these problems may be seen in U.S. Pat. No. 4,659,967 issued on Apr. 21, 1987 to Dahl; U.S. Pat. No. 5,111,195 issued on May 5, 1992 to Fukuoka et al.; U.S. Pat. No. 5,250,939 issued on Oct. 5, 1993 to Takanashi; U.S. Pat. No. 5,325,106 issued on Jun. 28, 1994 to Bahraman; U.S. Pat. No. 5,363,118 issued on Nov. 8, 1994 to Okumura; U.S. Pat. No. 5,426,430 issued on Jun. 20, 1995 to Schlig; U.S. Patent No. 5,523,772 issued on Jun. 4, 1996 to Lee; U.S. Pat. No. 5,572,211 issued on Nov. 5, 1996 to Erhart et al.; U.S. Pat. No. 5,574,475 issued on Nov. 12, 1996 to Callahan, Jr. et al. and U.S. Pat. No. 5,633,651 issued on May 27, 1997 to Carvajal et al.

U.S. Pat. No. 6,097,360 issued on August 1, 2000 to Holloman and U.S. Pat. No. 6,288,696 issued on September 11, 2001 to Holloman describe an analog-based approach for driving LEDs based upon a video signal. As set forth in those references, a sample-and-hold circuit is used to sample the video signal for each LED at its appropriate time during the frame interval. Each driver drives a respective LED with a current that is determined by the voltage level stored in the sample-and-hold circuit. A typical circuit as described in these patents may be seen at Fig. 1, discussed in some detail below.

As mentioned above, yet another problem is that many, if not most, prior-art approaches fail to address the problem that LEDs vary in brightness (as a function of drive current) and are non-uniform in wavelength (color). It is desirable to provide a means to compensate for the variations of intensity and color of LEDs which occur during their manufacturing processes. If the LEDs were assembled into an array as they were manufactured, the array field would have intensity variations that make the array look mottled, and there would be color variations in the array. It is a simple matter to adjust the currents in the LEDs to make the intensities uniform, but the assembly process then becomes very costly.

Merely controlling the current passing through the LEDs does not, however, suffice to adjust for the variations in color. Instead, companion colors must be added in near proximity to the display color on a per-pixel basis to compensate for the manufacturing variations. When the display is required to have the LEDs operate at variable intensities, the magnitude of companion colors that must be added must also vary in intensity. When the three primary LED colors of Red, Green and Blue are combined to make a full color display, each of these colors must be corrected to reproduce the original intended color faithfully.

One way to try to address these problems is by sorting LEDs so as to accumulate large quantities of LEDs with nearly identical characteristics. This requires applying a known current to each LED and performing measurements on the LED. One option is to test loose LEDs and to sort them based upon the measured characteristics of each LED. Such testing and sorting is expensive. Sorting based solely upon brightness would leave unaddressed the problem of color variations among LEDs. Sorting based upon brightness *and upon color* would lead to a need to sort into an extremely large number of bins. For example, sorting to provide six bits of resolution so far as brightness is concerned would require 64 bins. As described in more detail below, sorting to provide chrominance correction of similar resolution (with two degrees of freedom) would require 4096 bins for each of 64 brightness values. This would call for sorting into about a quarter of a million bins.

It will be readily appreciated that sorting into a quarter of a million bins is awkward and likely unworkable. Even if such sorting could be done economically, it would be necessary to carry out enough sorting so that one particular bin contains enough LEDs for a particular display to be manufactured. This might involve sorting (and then discarding for other uses) extremely large numbers of LEDs simply to arrive at a bin that contains enough LEDs for the display.

Yet another way to try to address these problems is to mount LEDs to circuit boards, to apply a known current to the LEDs, and then to perform measurements on the brightness and color of the LEDs one by one. The data resulting from the measurements must be stored for later use. Later

the circuit boards are tiled together to form a display of desired dimensions. It can then be proposed to perform digital calculations to try to correct luminance and chrominance. For example if an entire video frame is "grabbed" by a frame grabber, one proposed approach is to perform digital calculations upon the entire data set associated with the frame, prior to passing the data set to registers which control the pulse-width-modulated driving of the LEDs.

What will then be appreciated is that if luminance and chrominance correction calculations are to be performed digitally on a frame-by-frame basis, it is crucial to keep close track of which circuit board ended up where in the display. Once the tile locations of the circuit boards are determined, a data set must be assembled which contains all the various correction data in an order that corresponds to the tile positions.

Such an approach requires that a large body of data relating to the corrections be stored somewhere, generally in digital equipment that is separate from the display itself, and connected to the display by cabling. Such an approach faces possible difficulties. A first possible difficulty arises at the time the display is being assembled from its circuit boards; it might happen that the manufacturer could lose track of which circuit board ended up in which location within the display. This could lead to a difficulty that the data set containing the correction data would fail to match the display. In such a case, incorrect correction factors would be applied to some groups of LEDs, leading to a worsening in the visible variations of brightness and color. This could be generally termed a "data management" issue.

A second possible difficulty arises if the display needs to have one of its circuit boards replaced (for example as a repair or maintenance matter). If such a replacement occurs, the new LEDs will not match the brightness and color of the LEDs being replaced. If luminance and chrominance corrections are to be made for the new LEDs, this requires updating the data set for the display. If mistakes were made in such an update, then the display would get worse instead of better.

It would be very desirable if a way could be found to deal with manufacturing variations among LEDs, both as to brightness and as to chrominance, that is not prohibitively expensive, that achieves good results for human observers, and that avoids problems arising from data management issues.

SUMMARY OF THE INVENTION

A system is used with pixels, each pixel having at least three light-emitting diodes of at least three distinct colors. A driver chip is used which has, for each diode in the pixel, a sample-and-hold circuit which samples an analog video signal for the diode. A luminance-correction circuit draws upon a stored digital luminance correction factor and applies a luminance correction to the driver, the luminance correction factor being stored contiguous to the pixels. A chrominance-correction circuit draws upon stored digital chrominance correction factors for a diode in the pixel and upon signals indicative of the held signals for the other diodes in the pixel, and applies a chrominance correction to the driver input. The chrominance correction factors are also stored contiguous to the pixels.

DESCRIPTION OF THE DRAWING

The invention will be described with respect to a drawing in several figures.

Fig. 1 shows a prior-art LED driver circuit.

Fig. 2 shows an LED driver according to the invention.

Figs. 3A, 3B, 4A, and 4B show resistor ladders which may be used in a driver such as that of Fig. 2.

Fig. 5A shows modules 101 assembled into panels 102 which are in turn assembled into a

display 103.

Fig. 5B shows an integrated circuit chip 63 which drives eight pixels.

Fig. 5C shows the integrated circuit chip 63 of Fig. 5B with a different grouping of elements.

Fig. 6A shows propagation logic 107 of integrated circuit chip 63 in greater detail.

Fig. 6B shows how the chips 63 are interconnected so as to receive dot clocks and row-advance signals.

Figure 7 depicts one of the color channels of the circuitry of Fig. 2.

Fig. 8 shows a resistor ladder such as is shown in Figs. 3A, 3B, 4A, and 4B in greater detail and with an optional negative correction capability.

Fig. 9 shows in tabular form a set of computations for chrominance correction factors.

Where possible, like elements have been designated with like reference designations.

DETAILED DESCRIPTION

Fig. 1 shows a prior-art LED driver circuit such as that shown in the above-mentioned U.S. Pat. No. 6,097,360 issued on August 1, 2000 to Holloman and U.S. Pat. No. 6,288,696 issued on September 11, 2001 to Holloman, which patents are hereby incorporated herein by reference. The circuit relates to a single pixel 100 made up of three LEDs 100R, 100G, and 100R. This particular pixel 100 is assumed to lie at some particular location in a raster scanning pattern.

Video inputs 40R, 40G, and 40B may be seen at the right side of Fig. 1. These are analog video

signals, the amplitude of which would be used in a raster-scanned CRT display to "paint" color images on the phosphor screen.

Strobe line 16 is triggered at a time that corresponds to the raster-scanning interval for the particular location of the pixel 100 in the raster scanning pattern. Such strobing is accomplished with circuitry that is well known to those skilled in the art and the particular way selected to develop such strobe signals does not play part of the invention.

When the strobe line 16 is turned on (which is for a time interval corresponding to the pixel's location in the raster scanning pattern) then capacitors 18R, 18G, and 18B get charged to a voltage matching the voltage during the strobe interval. The capacitors are charged through switches 12R, 12G, and 12B which are preferably FETs (field-effect transistors).

The FETs and capacitors comprise "sample-and-hold" circuits, one for each of the three colors.

Each LED 100 is driven by a respective driver 10. Driver 10R, for example, is made up of amplifier 20R and FET 22R. Each driver provides current to its respective LED in proportion to the voltage stored in the respective storage capacitor.

For an array with, say, 320 by 256 pixels (that is, 81920 pixels), there would be 81920 drivers such as are shown in Fig. 1. The video signals 40 are connected in parallel to all of the 81920 drivers. Each driver 10 is strobed via its individual strobe line 16 at an appropriate time during the raster scanning pattern.

It will be appreciated that the circuit of Fig. 1 does not address luminance variations among LEDs, nor does it address chrominance variations among LEDs.

Fig. 2 shows an LED driver 67 according to the invention. The driver 67 is associated with a particular pixel composed of LEDs 100R, 100G, and 100B. For an array with, say, 320 by 256

pixels (that is, 81920 pixels), there would be 81920 drivers such as are shown in Fig. 2. The video signals 40 are connected in parallel to all of the 81920 drivers. Each driver 67 is strobed via its individual strobe line 16 at an appropriate time during the raster scanning pattern.

Switches 12 (preferably FETS) together with storage capacitors 10 make up "sample-and-hold" circuits, one for each of the three colors red, green, and blue. The sample-and-hold circuits function much like those in Fig. 1.

Amplifiers 22 and transistors 42 (preferably FETs) act as drivers for the LEDs 100. The drives are somewhat similar in function to the drivers 10 of Fig. 1, but as described below there is luminance-correction circuitry which interacts with the drivers.

As will be described in more detail below, in accordance with the invention there are measurements performed upon each pixel during the manufacturing process, yielding three correction factors for each LED in the pixel. For example for the red LED in a pixel, a first correction factor relates to luminance, a second correction factor relates to the green signal in the pixel, and a third correction factor relates to the blue signal in the pixel. As there are three LEDs in the pixel, each having three correction factors, thus there are a total of nine correction factors for each pixel.

As an example, for an array with, say, 320 by 256 pixels (that is, 81920 pixels), there would be 81920 drivers, each having nine correction factors, thus amounting to 737280 correction factors. In an exemplary embodiment, each correction factor is six bits, and thus the correction factors for such an array amount to some four megabits of correction-factor data. Importantly, as described below, in one embodiment of the invention the correction data is distributed with the drivers, for example 24 bits at a time.

The exemplary luminance-correction circuitry will now be discussed. Returning to Fig. 2, circuitry 53R relates to luminance correction for the particular LED 100R. A previously stored

luminance correction value is loaded into circuitry 53R by means of a data link omitted for clarity in Fig. 2.

Turning to Fig. 4B, the luminance correction circuitry 53 is shown. It takes as its input an input voltage and yields as its output a current signal. As is detailed in Fig. 4A, the circuitry includes a so-called R2R ladder. The ladder includes switches 68-0 through 68-5 which are set based upon the binary values of the luminance correction factor for the corresponding LED. One way to describe the resistor ladder is that it serves as a voltage divider, developing a voltage (and thus a current) that is a particular fraction of the input voltage. Another way to describe the ladder is that it applies a coefficient having a value between 0 and 1 to the input voltage.

Returning to Fig. 2, the current output of ladder 53R is summed with other currents at node 55R, and the summed currents provide the inverting input of amplifier 22R. As such, it affects the feedback for amplifier 22R. In this way it is possible to correct for brightness variations in the LEDs 100R.

Experience with LEDs teaches that a six-bit correction factor suffices to provide very good luminance correction. Employment of luminance correction as described herein across all of the LEDs of a particular color (say, red) leads to a situation where the actual brightness of the LEDs will be nearly constant across all LEDs if a constant video input voltage 40R is provided.

The exemplary chrominance-correction circuitry 51 will now be discussed. This circuitry 51 may be seen in Fig. 2. Circuitry 51RG and 51RB relates to chrominance correction for the particular LED 100R. A first previously stored chrominance correction value is loaded into circuitry 51RG by means of a data link omitted for clarity in Fig. 2. A second previously stored luminance correction value is loaded into circuitry 51RB by means of a data link omitted for clarity in Fig. 2. The first chrominance correction value relates to the extent to which the green signal 40G needs to be taken into account for the red LED 100R. The second chrominance correction value relates to the extent to which the blue signal 40B needs to be taken into account for the red LED

100R.

Node 52R will now be discussed in connection with chrominance correction. Node 52R represents a place where three currents are added together to perform a mathematical addition. Amplifier 50R provides a current proportional to the stored input at capacitor 18R. Circuitry 51RG provides a current proportional to the green signal, multiplied by the coefficient of the first luminance correction value. Circuitry 51RB provides a current proportional to the blue signal, multiplied by the coefficient of the second luminance correction value. These three currents are added and provide an input to amplifier 54R.

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The chrominance-correction circuity relating to the green LED 100G and the blue LED 100B function similarly. Correction coefficients are loaded into circuitry 51GR, 51GB, 51BG, and 51BR. For each of the LEDs, respective correction values relate to the extent to which the signals for the other two colors need to be taken into account.

Turning to Fig. 3B, the luminance correction circuitry 51 is shown. It takes as its input an input voltage and yields as its output a current signal. As is detailed in Fig. 3A, the circuitry includes a so-called R2R ladder. The ladder includes switches 69-0 through 69-5 which are set based upon the binary values of the one of the luminance correction factors for the corresponding LED.

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Returning to Fig. 2, the current outputs of ladders 51RG and 51RB are summed with other currents at node 52R, and the summed currents provide the inverting input of amplifier 54R. In this way it is possible to correct for color variations in the LEDs 100R.

Experience with LEDs teaches that two six-bit correction factors suffice to provide very good chrominance correction. Employment of chrominance correction as described herein across all of the LEDs of the pixels leads to a situation where the color rendering of the LEDs will be nearly consistent across all pixels if a constant video input voltage 40R, 40G, 40B is provided.

It is instructive to discuss the typical physical arrangements for the LEDs and for the drivers as well as digital logic employed with respect to a dot clock and row advance signals.

In an exemplary embodiment, for each pixel there are three LEDs, packaged in a very small square package, 0.120 inches on a side. For some data displays, it is unwise to closely pack the LEDs; they are usually clustered, with gaps between pixels for definition. Again in the exemplary embodiment, 16 rows of 16 pixels per row are placed on a small printed circuit board at 0.3 inch spacing, comprising what will herein be referred to as a "module" 101 shown in Fig. 5A.

Twenty-five modules 101 are then joined in a five-by-five array to form what will herein be referred to as a "panel" 102 shown in Fig. A. Each panel 102 has 80 rows and 80 columns of pixels.

Forty-eight panels 102 are then joined in an eight-by-six array to form a display 103 which is 640 by 480 pixels.

In this exemplary embodiment, the external signals driving the display 103 can be the same signals as are used in a computer system to drive a CRT display, such as a VGA display.

It should be appreciated that while this display 103 is shown as being 640 by 480 pixels, the invention is not so limited. The display can have a different number of rows or columns of pixels without departing from the invention. Likewise while this display 103 is described with a "pitch" (spacing between pixels) of 0.3 inch, other spacings may be used without departing from the invention.

It is convenient to provide integrated circuit chips 63 (Fig. 5B) each of which provides LED drive circuitry for eight pixels. Each pixels has three LEDs and thus the chip 63 has twenty-four circuits such as those shown in Fig. 7 or, stated differently, the chip 63 has eight circuits such as

those shown in Fig. 2. As shown in Fig. 5B, the chip 63 receives three analog video input signals 40R, 40G, and 40B. The video signal 40R is received by eight red intensity control blocks 106R each of which is circuit 67R in Fig. 2. Similarly the video signal 40G is received by eight green intensity control blocks 106G each of which is circuit 67G in Fig. 2. Finally the video signal 40B is received by eight blue intensity control blocks 106B each of which is circuit 67B in Fig. 2. Propagation logic 107 is provided, about which more will be said below. In this embodiment the chip 63 is a 64-pin package.

It should be appreciated that while the chip 63 is shown providing circuitry to drive eight pixels, the invention is not so limited and it would be possible to arrange such chips to drive some other number of pixels per chip. Experience suggests, however, that eight pixels is a convenient number of pixels per chip.

Returning to Fig. 5A, recall that module 101 has a 16-by-16 array of pixels, thus comprising 256 pixels. Because (in this embodiment) each chip 63 is able to drive eight pixels, it follows that thirty-two chips 63 must be included in each module 101. For each module 101, the LEDs are mounted on the front of the circuit board while the chips 63 are mounted on the reverse side for a total of 32 chips 63. One small connector (omitted for clarity in Fig. 5B) is mounted on the reverse side of module 101 for signal distribution.

As mentioned above, in an exemplary embodiment each pixel has three luminance correction factors of six bits each and six chrominance correction factors of six bits each, totaling fifty-four bits of correction data per pixel. Each chip 63 as portrayed in Fig. 5B drives eight pixels, and thus each chip 63 must store (either internally or in a contiguous memory) 432 bits of data. As a matter of design choice the 432 bits of memory are preferably nonvolatile. Each module 101 has 256 pixels, each of which has 54 bits of correction data, amounting to 13,824 bits per module 101.

One way to provide the memory is to include it as part of the integrated circuit chip 63. Another

way to provide the memory is on the module 101 (Fig. 5A) but external to the chips 63. In the latter case a memory chip of suitable capacity is mounted to the reverse side of the circuit board of the module 101. In either case the stored correction data will automatically follow the LEDs to which the data pertain.

The benefits of the above-mentioned approach (storing the correction factors contiguous with the associated LEDs) can now be clearly appreciated. When a particular module 101 is assembled it includes its LEDs. It also includes the nonvolatile memory which will store correction factors, either integral with driver chip 63 or in a separate chip that is also mounted to the circuit board 101. In this way it may be said that the correction values are stored contiguously with the LEDs and contiguously with the driver circuitry. Non-contiguous storage, namely storage where the correction values do not automatically "follow" the driver circuitry and the LEDs, would fail to offer benefits described herein.

After the module 101 has been assembled, a calibration procedure is performed. For each of the LEDs, one by one, a known voltage is presented at the associated capacitor 18, thereby illuminating the LED. For each illuminated LED, the brightness is measured. Color measurements are performed for each of the three LEDs in a pixel. As will be described below, correction factors are derived from the measurements. Importantly, the correction factors are then stored in the nonvolatile memory of the module 101, which completes the calibration procedure.

When modules 101 are assembled together to form a display 103, what is important is that the correction factors associated with a particular set of LEDs will follow the LEDs. There is no need to keep track of which module 101 ends up in a particular position. Instead, no matter where a particular module 101 is placed, the correction factors for the LEDs of that module 101 will be in the correct location.

Likewise, if a module gets replaced after manufacture, for example due to a maintenance or repair procedure, the new module will carry its correction factors with it (because the correction factors are physically contiguous with the LEDs associated therewith). Luminance and chrominance correction are preserved in a simple and nearly foolproof way. There are few if any "data management" issues as there are if such corrections are performed by means of digital calculations.

Turning now to Fig. 5C, what is shown is the integrated circuit chip 63 with functional elements grouped differently than as portrayed in Fig. 5B. In Fig. 5C, each pixel 100 (comprising three LEDs) is driven by circuitry 67 (also shown in Fig. 2). Eight circuits 67 are shown, and these circuits 67 receive (in parallel) the analog video signals 40R, 40G, and 40B.

By way of larger perspective with respect to Fig. 5A, as will be appreciated, the analog video signals 40R, 40G, and 40B are provided to the display 103, which in turn provides the analog video signals 40R, 40G, and 40B in parallel to all of the panels 102 (here, 48 panels). Each panel 102 provides the analog video signals 40R, 40G, and 40B in parallel to each of its modules 101 (here, twenty-five modules). Each module 101 provides the analog video signals 40R, 40G, and 40B in parallel to each of its integrated circuit chips 63 (here, thirty-two chips). Finally, each chip 63 provides the analog video signals 40R, 40G, and 40B in parallel to each of its drivers 67 (here, eight drivers).

Returning to Fig. 5C, it is appreciated that each driver 67 needs to know when, exactly, it should trigger its sample-and-hold circuitry to capture the analog video signals 40R, 40G, and 40B. Stated differently with respect to Fig. 2, each driver 67 needs to know when, exactly, it should trigger its transistors 12. In Fig. 2 this trigger is communicated on line 16. In Fig. 5C the lines 16 are shown, and they are eight in number, one for each driver 67, and they are provided by decoder 105. Decoder 105 is in turn controlled by synch counter 61. Decoder 105, synch counter 61, and related circuitry are collectively termed propagation logic 107, previously mentioned in connection with Fig. 5B.

Returning again to Fig. 5C, one of the inputs is a dot clock 108. This clock "ticks" once for each pixel time. In a 640 by 480 display, this clock will "tick" some 307,200 times for each refresh interval. It will be appreciated that a particular chip 63 (containing drivers for eight particular pixels out of 307,200 pixels) is only interested in eight of the "ticks". A load signal 114 allows the chip 63 to know that its eight interesting "ticks" are about to happen. The eight "ticks" cause synch counter 61 to count from 0 to 7, and the "carry" bit (indicative that eight ticks have been counted) defines the load extend signal 109. As will be described in more detail, the load extend signal 109 is connected to an appropriate pin on the "next" chip 63 so that it may know when the eight ticks that are of interest will arrive. In this way the chips 63 for a particular display row are daisy-chained, each chip 63 paying attention to eight ticks associated with its eight pixels, and each chip 63 notifying its neighbor that its turn has arrived.

The decoder 105 is a standard 3-to-8 decoder, receiving a three-digit binary number from synch counter 61 and emitting in turn a trigger on each of the eight lines 16.

Fig. 6A shows the propagation logic 107 in greater detail. The dot clock 108 is provided to a particular chip 63 and indeed is provided in parallel to all of the chips 63, in much the same way that the analog color signals are provided in parallel to all of the chips 63 as mentioned above. A row advance signal 112 is provided from an external source, and this signal happens once per row of the display 103 (Fig. 5A). Thus in a display with 480 rows, the row-advance signal 112 will trigger 480 times per display refresh interval.

In Fig. 6A, when a particular chip 63 is enabled by means of enable line 110, then the dot clocks of line 108 cause the counter 61 to count for eight dot clocks. After eight counts the load extend signal 109 is generated which enables the "next" chip 63. The row advance signal 112 and row enable extend signal 111 are shown and will be discussed in connection with Fig. 6B.

Fig. 6B depicts a 640 by 480 display 103 (Fig. 5A) in greater detail, showing the interconnections between the chips 63. The display 103 has 480 rows of pixels and, correspondingly, Fig. 6B

shows 480 rows of chips 63. The display 103 has 640 columns of pixels, and each chip 63 drives eight of the pixels, thus there are eighty chips 63 in each row. The total number of chips 63 portrayed in Fig. 6B is thus eighty times 480 or 38,400.

Each of the chips 63 needs to know when its particular eight dot clicks occurs. With the exception of the topmost and leftmost chip 63A, each chip 63 is enabled by some previous chip 63 in the array. Chip 63B, for example, gets its enable signal 110 (shown in Fig. 6A) from the load extend signal 109 (shown in Fig. 6A) of chip 63A. In the same way the load extend and enable signals propagate along the first row to the rightmost chip 63 in the row. In this way, 640 dot clocks are received by chips 63 for the 640 pixels in the row.

Once the first row (Fig. 6B) has been loaded with its 640 analog values for its 640 pixels, the row advance signal 112 indicates that the analog video data now being provided relate to the second row in Fig. 6B. As shown in Fig. 6A, the row advance signal 112 is received and a row enable extend signal 111 is generated. As shown in Fig. 6B, the chips 63 in the first column pass the row enable extend signals 111 downward in the first column, each such signal being received as an enable signal 110 for the chip 63 that is below. In this way the row advance signals 112 suffice to step through the rows of the display until the last row (here, the 480-th row) has received its 640 dot clocks.

Omitted for clarity in Fig. 6B are the three analog video signals 40R, 40G, 40B as well as the dot clock 108, all of which are provided in parallel to all of the chips 63 in Fig. 6B.

The cabling and/or connectors of an exemplary embodiment will now be briefly described. Each module 101 will have a cable or connector connecting it to a panel 102. This cable will receive about a dozen signals — three analog video signals, a dot clock, a row advance signal, a chip-enable signal, power signals, and optionally a reset signal and a clear signal. It will carry about two dozen signals to the panel 102 — about sixteen row-enable extend signals and a load extend signal. It will be appreciated that this is a relatively small number of signals when one considers

the large number of states to be controlled and maintained within the module.

In this exemplary embodiment each panel 102 will likewise have a cable or connector connecting it to the display 103. This cable will also carry a relatively small number of signals by comparison with the number of states to be controlled and maintained. This cable will receive about a dozen signals — three analog video signals, a dot clock, a row advance signal, a chip-enable signal, power signals, and optionally a reset signal and a clear signal. It will carry about eighty-one signals to the panel 102 — about eighty row-enable extend signals and a load extend signal.

Most advantageously the cables or connectors connecting the modules 101 to the panels 102, and connecting the panels 102 to the display 103, have only modest bandwidth requirements. The video signals are the highest-bandwidth signals being propagated and the dot clock is the highest-frequency digital signal being propagated, but these signals are no more difficult to propagate than in other applications such as LCD screens and CRT screens. This is in contrast to some other approaches for driving and controlling LED-array screens in which information must be passed in high-bandwidth digital links to control PWM drivers for individual LEDs.

It will be appreciated that so far as the luminance- and chrominance-correction aspects of the invention are concerned, it is immaterial precisely how the propagation-logic signals are processed and acted upon. The precise number of rows and columns of a display, the dot clock interval, the row advance interval, and the screen refresh interval are all immaterial to such luminance- and chrominance-correction aspects of the invention. Likewise there can be a vertical blanking interval and/or a horizontal retrace interval, and if there are such intervals, the duration of such intervals is immaterial to such luminance- and chrominance-correction aspects of the invention. The video information being displayed can be NTSC, PAL, SECAM, or other format without departing from the teachings of the invention with respect to the luminance- and chrominance-correction aspects of the invention. Finally, while many analog video signals are in a range of 0 to 1 volt, it should be appreciated that the signals could be provided over some other

range with suitable modification of the gains of the input stages that receive those signals.

The mathematics of luminance and chrominance correction for LEDs will now be discussed.

The NTSC specifications for the CRT phosphors on the C.I.E. 1931 Chromaticy Diagram, along with their relative intensities for a 6500K White balance, are as follows:

Red	x=0.67,	y=0.33	I = 2.76732532
Green	x=0.21,	y=0.71	I = 5.78998150
Blue	x=0.14.	y=0.08	I = 1.00000000
White	x=0.3127,	y=0.3291	6500K

Experience with high-quality LEDs from a typical vendor leads to an appreciation that there are manufacturing variations which cause the color coordinates of the LEDs to vary, as well as the intensity of the emitted light. Both the color coordinates (Chroma) and the intensities (Luminance) ratios must be adjusted to produce the full color gamut.

For a particular vendor of LEDs, a typical expected variation of color coordinates is:

Red LED	x= 0.67 - 0.73,	y= 0.27 - 0.33
Green LED	x= 0.14 - 0.22,	y= 0.64 - 0.74
Blue LED	x= 0.11 - 0.15,	y= 0.04 - 0.10

Intensity variations can be over a range of as much as 2:1 depending on quality control.

The red x coordinate can be pulled from 0.73 to the NTSC standard of 0.67 by adding either Blue, Green or both in some percentage. The 0.27 y coordinate can be pulled to the 0.33 NTSC standard by adding only green, but not blue.

The green x coordinate of 0.14 can be pulled up to 0.21 by adding red. The 0.22 coordinate can be pulled down to 0.21 by adding blue. The 0.64 y coordinate cannot be raised by adding either red or blue, only by subtracting some red or blue if the red or blue LED was on. The 0.74 y coordinate can be pulled down by adding blue or red.

The blue x coordinate of 0.11 can be pulled to the NTSC standard of 0.14 by adding red. The 0.15 coordinate cannot be pulled down by adding green, but only by subtracting green if the LED were on. The 0.04 coordinate can be pulled up to the NTSC standard of 0.08 by adding green, but the 0.10 coordinate can only be pushed down by subtracting green, or red.

The calculations for determining the percentage of red, green and blue LED intensities to add to make the correction is rather straightforward and defined by C.I.E. In 1931. The calculations for a typical example are provided in Table 9.

If the colors are to be accurate and that a field of red, green or blue is to appear uniform to the human eye, then the general requirements after compensation may be:

- The intensity ratios should vary less than 10 percent from calculated values.

- The red color which had an initial variation from 615nm to 635nm should be corrected to within 4 nm.

- The green color which had an initial variation from 520nm to 535nm should be corrected to within 3 nm.

- The blue color which had an initial variation from 464nm to 475nm should be corrected to within 2 nm.

Typically the LEDs will be sorted to the best selection available and mounted on a pixel array,

perhaps 16 by 16 for convenience. Each pixel is then illuminated one PEL (one LED) at a time and their x, y and I values measured and stored in a memory. The intensities must next be adjusted to obtain the intended balance between red, green and blue for white balance control, and must also be adjusted so that each LED color meets a calculated intensity which all, or the majority of the LEDs can meet. If the selection of the LEDs were performed well, then the LED correction of any PEL should be within 1.5 to 1. (The system should be capable of adjusting for a 2:1 variation.)

The only drive parameter for an LED which the system designer can control is the current into the LED. Within its normal operating range, the intensity of the LED will be directly proportional to the current. The intensity of the LED for display is determined by the analog value of the video signal for red, green or blue, and the LED current is directly proportional to the video voltage in the analog driver system. For a system designer, if a correction to the LED drive system is to be made, the correction must be either a variation of the video drive voltage, or must be a control of the gain of the feedback resistor comparator. In an exemplary embodiment, all intensity compensations are accomplished by controlling the gain of the feedback resistor comparator.

If, for example, it is needed to correct the red color coordinates by adding blue, then it is necessary to increase the blue LED current. If blue is not called for in this particular pixel, then the blue LED must be turned on by the correction circuitry. It is only possible to subtract a color if that color had been called for in the video display signal. If that LED is not on, then a negative correction cannot be made. This may, or may not be consequential in real pixels made with real LEDs. In general, to correct for red, calculated percentages of green and blue are added, whether it be positive or negative, in proportion of the intensity of the red to be displayed. The corrections for green and blue are calculated and are then summed with the red display values and the red LED is driven with a constant current driver for that LED. Similarly, the green display value and its corrections are summed, and the blue display value with its corrections are summed, and are presented to their respective analog constant current LED drivers.

One LED and its associated driver is shown in Figure 7, which depicts one of the color channels of the circuitry of Fig. 2. The function of the driver will now be described in greater detail.

The value to be displayed is stored on capacitor 18 by the sample-and-hold control circuitry 12. OpAmp 50 is used to isolate and buffer the stored display value. The stored value is converted to current by resistor 2R (81) which drives current into junction 52. The stored display value is presented through lead 82 to PEL 2 and through lead 83 to PEL 3 for use in their respective correction circuitry. The display value from PEL 2 is presented to the R2R ladder 51 over lead 84, and its current output drives current into the summing junction 52 through lead 85. The display value 86 from PEL 3 drives current into junction 52 through lead 87 in a similar manner. The output voltage 88 from the current-to-voltage converter 54 draws an equal amount of current out of junction 52 as that the sum of the currents must be zero, and its negative voltage 88 then is precisely the sum of the display voltage stored on capacitor 18, and the correction values 84, 86 from PEL 2 and PEL 3.

The negative voltage Eo 88 draws current out of junction 55 through resistor 89, and is connected to the negative input of amplifier 22 which turns the LED drive transistor 42 on, driving current through the LED 100 and resistor 30. The voltage developed through resistor 30 drives current into junction 55 through resistor 90. The voltage derived from the LED current is also connected to 6-bit R2R ladder 53, and its proportional output current I out also drives current into junction 55 so that the sum of the currents into junction 55 is precisely zero.

The resistor ladder networks will now be described in greater detail, and a variant of the resistor ladder providing an optional negative correction will be described, all with respect to Figs. 3A and 8.

Fig. 3A shows a classic R2R ladder network 51 where each 2R resistor is terminated in either ground or Iout 94, as directed by the 6-bit control signals 69-0 through 69-5. In this way the resistor network presents a constant impedance to the Vin signal 93. The Vin signal level 93 is

thus divided by two by each resistor R stage, and the resistors 2R convert that voltage to current. The current developed in the 2R resistors is selectively added to Iout 94 as directed by the 6 binary weighted control leads 69-0 through 69-5. The output voltage of Iout 94 is held at ground level by the current-summing junction (omitted for clarity in Fig. 3A) to which Iout 94 is connected.

The current out 94 is thus proportional to the product of the voltage in 93 and a six-bit binary constant provided on lines 69-0 through 69-5. Line 69-5 receives the most-significant bit (MSB) of the binary constant and line 69-0 receives the least-significant bit (LSB) of the binary constant.

Preferably the Chroma control R2R ladder 51 (Figs 2 and 3A) has the most-significant stage (resistor 95 in Fig. 3) connected to ground so that the remaining six stages have a finer resolution.

Those skilled in the art whose experience extends several decades into the past will appreciate that the circuitry of Fig. 2 may be understood as a group of analog computers, each computing sums and proportions of various signals to bring about the chrominance and luminance corrections.

Fig. 8 shows a variant of the resistor ladder such as that shown in Figs. 3A and 4A. In this embodiment, an analog inverter 97 is provided as shown. A switch 96 selects either the Vin signal 93, or its negative, as the input to the resistor ladder. In this way, an additional bit can be provided so that a seven-bit binary constant will be able to specify negative and positive correction values.
The table of Fig. 9 illustrates how the correction values are determined.

Column 1 lists the LED colors.

Columns 2 and 3 list the 1931 CIE color coordinates typical of NTSC-recommended phosphors

as used in cathode-ray tube (CRT) displays.

Column 4 lists the relative intensities of each color to obtain a 6500 K (Kelvin) white balance for the display.

Column 5 shows the display intensities to obtain a display with a brightness of 2000 candelas per square meter with a white balance of 6500 K.

Column 6 and 7 show examples of the LED coordinates used for this example of how typical commercial LEDs may be corrected to NTSC values. These values are examples of actual values that might be measured for LEDs selected randomly from the production of a well-known manufacturer of LEDs.

Column 8 lists the calculated relative intensities of these LEDs that would be required to produce a white balance of 6500 K.

Column 9 lists the LED intensities required to produce a display brightness of 2000 candelas per square meter.

Columns 10, 11, and 12 are the calculated correction ratios that must be applied to the respective colors to present the same color gamut as the NTSC-recommended phosphors. Since these values are fractions, the sum of each column equal unity (100%).

The red correction RED value (the "red" row for column 10) is the value for red after the luminance has been corrected to a reference standard.

The red correction GREEN value (the "green" row for column 10) is the value which will be stored in a non-volatile memory and presented to R2R RG (circuit 51GR in Fig. 2) for addition to the green display signal.

The red correction BLUE value (the "blue" row for column 10) is presented to R2R RB (circuit 51BR in Fig. 2).

Green Correction Red (the "red" row for column 11) is presented to R2R GR (circuit 51RG in Fig. 2).

Green Correction Blue (the "blue" row for column 11) is presented to R2R GB (circuit 51BG in Fig. 2).

Blue Correction Red (the "red" row for column 12) is presented to R2R BR (circuit 51RB in Fig. 2).

Blue Correction Green (the "green" row for column 12) is presented to R2R BG (circuit 51GB in Fig. 2).

The calculations below the table of Fig. 9 are presented to demonstrate that when the corrections are made, the NTSC WHITE relative values which are the sums of their respective corrected values now precisely equal the calculated values in Column 8.

In our example of correcting typical LEDs to NTSC standards, the red correction of column 10 requires removing 1/3 percent of blue, which is below the normal correction threshold, and may be ignored. The green correction for blue (the "blue" row of column 11) is nearly 2/3 percent and may be considered. When negative corrections are required, then the negative value of the display value stored on capacitor 18 may be presented by adding an inverter 97 as shown on Fig 8.

In an exemplary embodiment, the amplifiers employed are operational amplifiers (op amps).

The circuits described here take as their starting point the drivers described in the above-

mentioned U.S. Pat. No. 6,097,360 issued on August 1, 2000 to Holloman and U.S. Pat. No. 6,288,696 issued on September 11, 2001 to Holloman. It should be appreciated, however, that without deviating in any way from the invention, it would be possible to replacing capacitor 18 (and its associated sample-and-hold circuitry 12, shown in Figs. 2 and 7) with a variable-voltage digital-to-analog converter (DAC). Likewise the sample-and-hold circuitry 12 and capacitor 18 (shown in Figs. 2 and 7) may be replaced with a fixed voltage which is switched from Ground to its fixed value by a serial digital data stream so that the actual display intensity may be controlled by a Pulse Width Modulation (PWM) system. Stated differently, even if the video input information is provided digitally rather than by means of an analog signal, the teachings of the invention may apply equally well to provide chrominance and luminance correction (or luminance correction alone).

It should be appreciated as well that the teachings of the invention with respect to luminance correction may be applied even if no chrominance correction is performed. Stated differently, it is also possible to operate the correction system with only the luminance control circuitry, singly or in combination with other colors so that one intensity of that LED may be set to a specified reference value. Again, the signal driving the final LED driver may be an analog voltage on a capacitor 18; a variable voltage from a DAC; or a fixed voltage controlled by a digital input data stream for PWM control of the display.

The invention has been described in the particular context of light-emitting diodes, and this is motivated by the prevalence of light-emitting diodes in present-day display screens. It should be appreciated, however, that the teachings of the present invention offer themselves for any of many types of light-emitting device, particularly those light-emitting devices that are monochromatic or emit only a small number of fixed wavelengths, and that emit light with a brightness that is substantially linear with respect to their electrical input.

While the invention has been described with respect to particular embodiments, the invention should not be understood as being limited to the particular embodiments. Indeed, those skilled in

the art will have no difficulty devising myriad obvious variations and enhancements of the invention without deviating from the invention's teachings in any way, and it is intended that all such variations and enhancements

CLAIMS

1. A method for use with an array of light-emitting devices, the method comprising the steps of:

passing a current through each device and measuring the brightness of each device;

deriving a luminance correction value for each device from the current and the measured brightness; and

storing digital information indicative of the luminance correction value for each device in a digital memory contiguous with the device.

2. The method of claim 1 further comprising the steps of:

sampling and holding an analog voltage indicative of a desired video drive for each device;

passing a current through each device as a function of the held voltage associated with the device;

applying a luminance correction factor for each device to the passed current through the device as a function of the stored digital information indicative of the luminance correction value for the device.

3. The method of claim 1 wherein the array comprises at least four light-emitting devices, and wherein the passing, deriving, and storing steps are performed respectively for each of the at least four devices, and wherein the stored digital information indicative of the luminance correction value for each device is stored in a single memory.

4. A method for use with an array of pixels, each pixel comprising light-emitting devices of at

least first, second, and third colors, the method comprising the steps of:

passing a current through each device and measuring the brightness of each device;

deriving a luminance correction value for each device from the current and the measured brightness; and

storing digital information indicative of the luminance correction value for each device in a digital memory contiguous with the device.

5. The method of claim 4 further comprising the steps of:

sampling and holding an analog voltage indicative of a desired video drive for each device;

passing a current through each device as a function of the held voltage associated with the device;

applying a luminance correction factor for each device to the passed current through the device as a function of the stored digital information indicative of the luminance correction value for the device.

6. The method of claim 4 wherein the array comprises at least four pixels, and wherein the passing, deriving, and storing steps are performed respectively for each device of the at least four pixels, and wherein the stored digital information indicative of the luminance correction value for each device is stored in a single memory.

7. The method of claim 4 further comprising the steps of:

for each pixel, passing currents through the devices of the pixel and measuring the deviation

from a reference color value associated with the pixel;

deriving chrominance correction factors for each pixel from the currents and the measured deviations; and

storing digital information indicative of the chrominance correction factors for each pixel in a memory contiguous with the pixel.

8. The method of claim 7 wherein the number of derived chrominance correction factors is at least n^2-n where n is the number of light-emitting devices per pixel.

9. The method of claim 8 wherein the number of derived chrominance correction factors is six and the number of light-emitting devices per pixel is three.

10. The method of claim 7 further comprising the steps of:

sampling and holding an analog voltage indicative of a desired video drive for each device;

passing a current through each device as a function of the held voltage associated with the device;

applying a luminance correction factor for each device to the passed current through the device as a function of the stored digital information indicative of the luminance correction value for the device; and

applying a chrominance correction factor for each device to the passed current through the device as a function of the stored digital information indicative of the chrominance correction value for the device and as a function of the held voltages for the other devices in the pixel.

11. The method of claim 7 wherein the array comprises at least four pixels, and wherein the passing, deriving, and storing steps are performed respectively for each device of the at least four pixels, and wherein the stored digital information indicative of the luminance correction value for each device and the chrominance correction values or each device is stored in a single memory.

12. A method for driving an array of light-emitting devices, the method comprising:

for each device, sampling and holding an analog voltage indicative of a desired video drive for the device;

for each device, passing a current through the device as a function of the held voltage associated with the device;

for each device, retrieving a stored digital luminance correction factor for the device from a digital memory contiguous with the array of devices;

for each device, applying the luminance correction factor for the device to the passed current through the device.

13. A method for driving an array of pixels, each pixel comprising at least first, second, and third light-emitting devices of differing colors, the method comprising:

for each device in a pixel, sampling and holding an analog voltage indicative of a desired video drive for the device;

for each device in a pixel, passing a current through the device as a function of the held voltage associated with the device;

for each device in a pixel, retrieving a stored digital luminance correction factor for the device

from a digital memory contiguous with the array of devices;

for each device in a pixel, applying the luminance correction factor for the device to the passed current through the device.

14. The method of claim 13 further comprising the steps of:

for each device in a pixel, retrieving digital chrominance correction factors for each device from the digital memory contiguous with the array of devices;

for each device in a pixel, applying the chrominance correction factors for each device with respect to the held voltage of the other devices in the pixel, to the passed current through the device.

15. Apparatus comprising:

a circuit board;

light-emitting devices mounted to the circuit board;

an integrated circuit chip mounted to the circuit board;

the chip comprising:

for each device, sample-and-hold means responsive to an analog video signal for the device, and responsive to a sample signal for sampling and holding the analog luminance signal;

for each device, a driver responsive to an input for driving the device to emit light;

for each device, a luminance-correction means responsive to a stored digital luminance correction factor for applying a luminance correction to the driver input;

for each device, the driver input comprising the luminance correction and a signal indicative of the held signal for the device.

16. The apparatus of claim 15 wherein the stored digital luminance correction factors are stored external to the chip.

17. The apparatus of claim 15 wherein the number of devices mounted to the circuit board is at least four.

18. The apparatus of claim 15 wherein the input to each driver is a current input, and wherein the luminance correction and the signal indicative of the held signal for the device comprise currents that are added to comprise the input to the driver.

19. The apparatus of claim 15 wherein each luminance-correction means comprises a resistor ladder responsive to bits of the digital luminance correction factor, the ladder serving as a voltage divider taking as its input a signal indicative of current through the respective device, and providing as its output a portion of that signal.

20. Apparatus comprising:

a circuit board;

pixels mounted to the circuit board, each pixel comprising at least three light-emitting devices of at least three distinct colors;

an integrated circuit chip mounted to the circuit board;

the chip comprising:

for each device in a pixel, sample-and-hold means responsive to an analog video signal for the device, and responsive to a sample signal for sampling and holding the analog luminance signal;

for each device in a pixel, a driver responsive to a input for driving the device to emit light;

for each device in a pixel, a luminance-correction means responsive to a stored digital luminance correction factor for applying a luminance correction to the driver input;

for each device in a pixel, a chrominance-correction means responsive to stored digital chrominance correction factors and responsive signals indicative of the held signals for the other devices in the pixel, for applying a chrominance correction to the driver input;

for each device in a pixel, the driver input comprising the luminance correction, the chrominance correction, and a signal indicative of the held signal for the device.

21. The apparatus of claim 20 wherein the stored digital luminance correction factors and stored digital chrominance correction factors are stored external to the chip.

22. The apparatus of claim 20 wherein the number of pixels mounted to the circuit board is at least four.

23. The apparatus of claim 20 wherein the input to each driver is a current input, and wherein the luminance correction and the chrominance correction and the signal indicative of the held signal for the device comprise currents that are added to comprise the input to the driver.

24. The apparatus of claim 20 wherein each luminance-correction means comprises a resistor ladder responsive to bits of the digital luminance correction factor, the ladder serving as a voltage

divider taking as its input a signal indicative of current through the respective device, and providing as its output a portion of that signal.

25. The apparatus of claim 20 wherein each chrominance-correction means comprises, for each other device in a pixel, a resistor ladder responsive to bits of the chrominance correction factor respective to each other device, the ladder serving as a voltage divider taking as its input a signal indicative of the held signal for the each other device, and providing as its output a portion of that signal.

26. An integrated circuit chip for use with devices, the chip comprising:

for each device, sample-and-hold means responsive to an analog video signal for the device, and responsive to a sample signal for sampling and holding the analog luminance signal;

for each device, a driver responsive to an input for driving the device to emit light;

for each device, a luminance-correction means responsive to a stored digital luminance correction factor for applying a luminance correction to the driver input;

for each device, the driver input comprising the luminance correction and a signal indicative of the held signal for the device.

27. The apparatus of claim 26 wherein the stored digital luminance correction factors are stored external to the chip.

28. The apparatus of claim 26 wherein the number of devices is at least four.

29. The apparatus of claim 26 wherein the input to each driver is a current input, and wherein the luminance correction and the signal indicative of the held signal for the device comprise currents

that are added to comprise the input to the driver.

30. The apparatus of claim 26 wherein each luminance-correction means comprises a resistor ladder responsive to bits of the digital luminance correction factor, the ladder serving as a voltage divider taking as its input a signal indicative of current through the respective device, and providing as its output a portion of that signal.

31. An integrated circuit chip for use with pixels, each pixel comprising at least three light-emitting devices of at least three distinct colors, the chip comprising:

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for each device in a pixel, sample-and-hold means responsive to an analog video signal for the device, and responsive to a sample signal for sampling and holding the analog luminance signal;

for each device in a pixel, a driver responsive to a input for driving the device to emit light;

for each device in a pixel, a luminance-correction means responsive to a stored digital luminance correction factor for applying a luminance correction to the driver input;

for each device in a pixel, a chrominance-correction means responsive to stored digital
20 chrominance correction factors and responsive signals indicative of the held signals for the other devices in the pixel, for applying a chrominance correction to the driver input;

for each device in a pixel, the driver input comprising the luminance correction, the chrominance correction, and a signal indicative of the held signal for the device.

32. The apparatus of claim 31 wherein the stored digital luminance correction factors and stored digital chrominance correction factors are stored external to the chip.

33. The apparatus of claim 31 wherein the number of pixels is at least four.

34. The apparatus of claim 31 wherein the input to each driver is a current input, and wherein the luminance correction and the chrominance correction and the signal indicative of the held signal for the device comprise currents that are added to comprise the input to the driver.

35. The apparatus of claim 31 wherein each luminance-correction means comprises a resistor ladder responsive to bits of the digital luminance correction factor, the ladder serving as a voltage divider taking as its input a signal indicative of current through the respective device, and providing as its output a portion of that signal.

36. The apparatus of claim 31 wherein each chrominance-correction means comprises, for each other device in a pixel, a resistor ladder responsive to bits of the chrominance correction factor respective to each other device, the ladder serving as a voltage divider taking as its input a signal indicative of the held signal for the each other device, and providing as its output a portion of that signal.

37. Apparatus for driving a light-emitting device, the apparatus comprising:

a driver responsive to an input for causing current to flow through the device;

a feedback means responsive to current through the device for providing feedback to the driver;

the feedback provided to the driver according to a value stored in a nonvolatile memory.

38. The apparatus of claim 37 wherein the nonvolatile memory is contiguous with the driver.

39. The apparatus of claim 37 further comprising the light-emitting device, the nonvolatile memory contiguous with the device.

40. The apparatus of claim 37 wherein the input is an analog voltage.

41. The apparatus of claim 37 wherein the input is a voltage stored on a capacitor.

42. The apparatus of claim 37 wherein the input is a fixed voltage modulated by a pulse-width modulation.

43. A method for driving a light-emitting device, the method comprising the steps of:

driving the device by a driver with current in response to an input;

responding to the current through the device by providing a feedback to the driver;

the feedback being provided according to a value stored in a nonvolatile memory contiguous with the device.

44. Apparatus comprising;

a plurality of light-emitting devices;

a driver corresponding to and connected with each of the light-emitting devices and disposed to pass current therethrough in response to a respective display intensity level input;

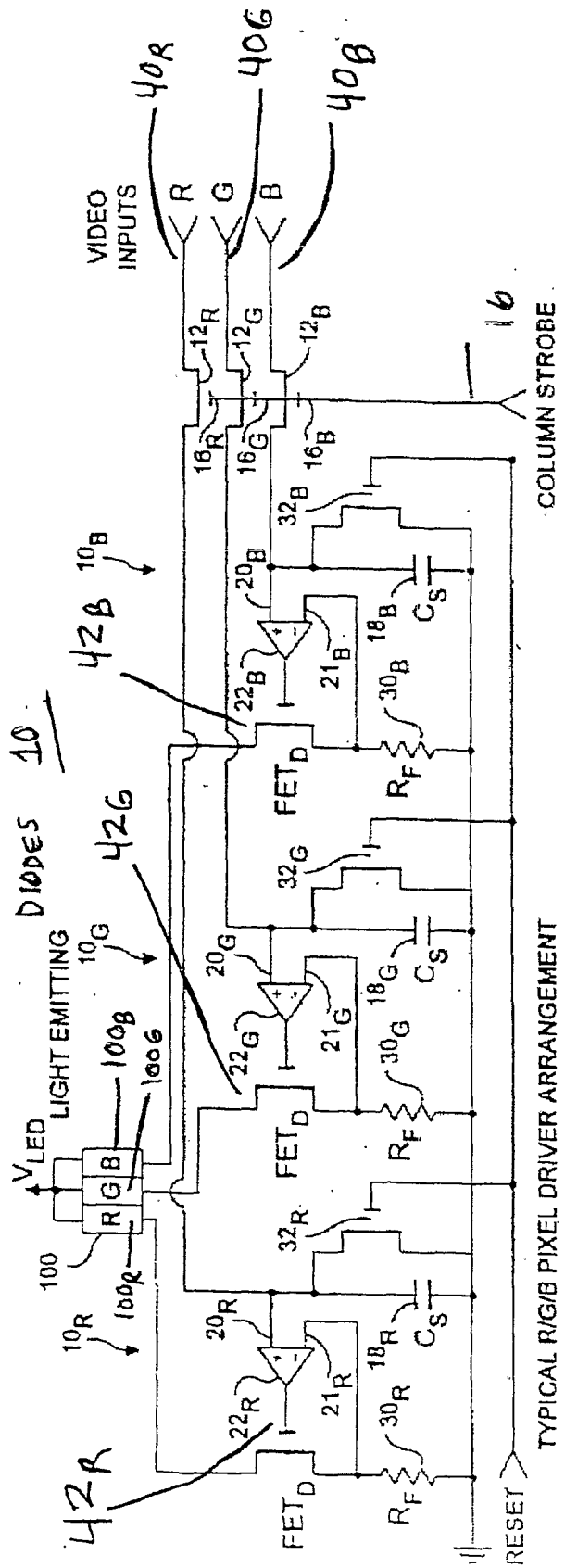
a feedback means corresponding to and connected with each of the light-emitting devices, the feedback means responsive to the current passing through the light-emitting device for providing feedback to the driver according to a value stored in a nonvolatile memory contiguous with the driver;

a correction means corresponding to each of the drivers, the correction means for each driver adding signals from the other drivers in proportion to values stored in nonvolatile memories contiguous with the driver.

45. The apparatus of claim 44 wherein each display intensity level input is an analog voltage.

46. The apparatus of claim 44 wherein each display intensity level input is a voltage stored on a capacitor.

47. The apparatus of claim 44 wherein each display intensity level input is a fixed voltage modulated by a pulse-width modulation.



PRIOR ART

Fig. 1

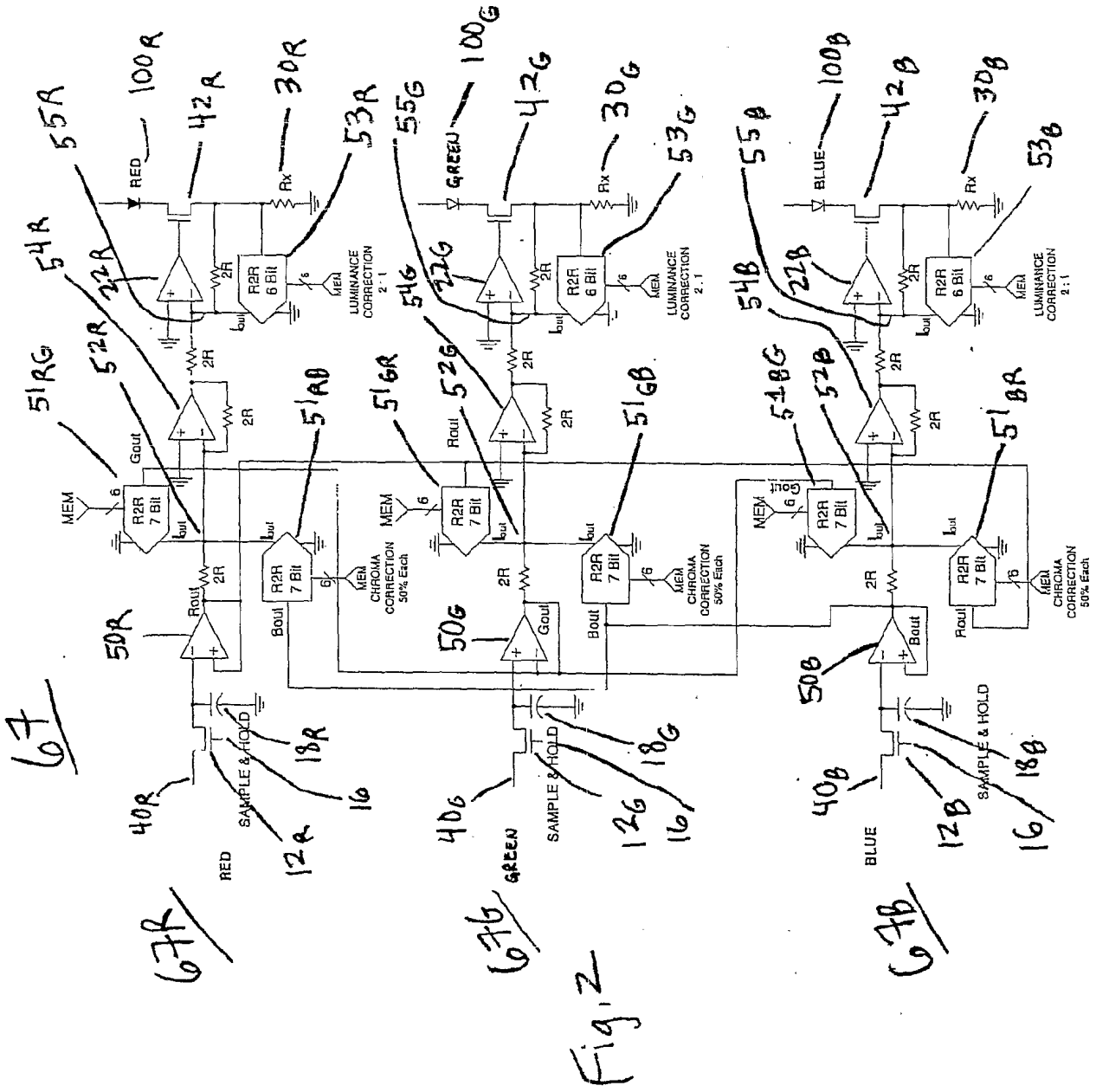

67
67R
67G
67B
RED
GREEN
BLUE
SAMPLE & HOLD
R2R 7 Bit
R2R 6 Bit
MEM
LUMINANCE CORRECTION 2:1
CHROMA CORRECTION 50% Each
Rx
2R

Fig. 2

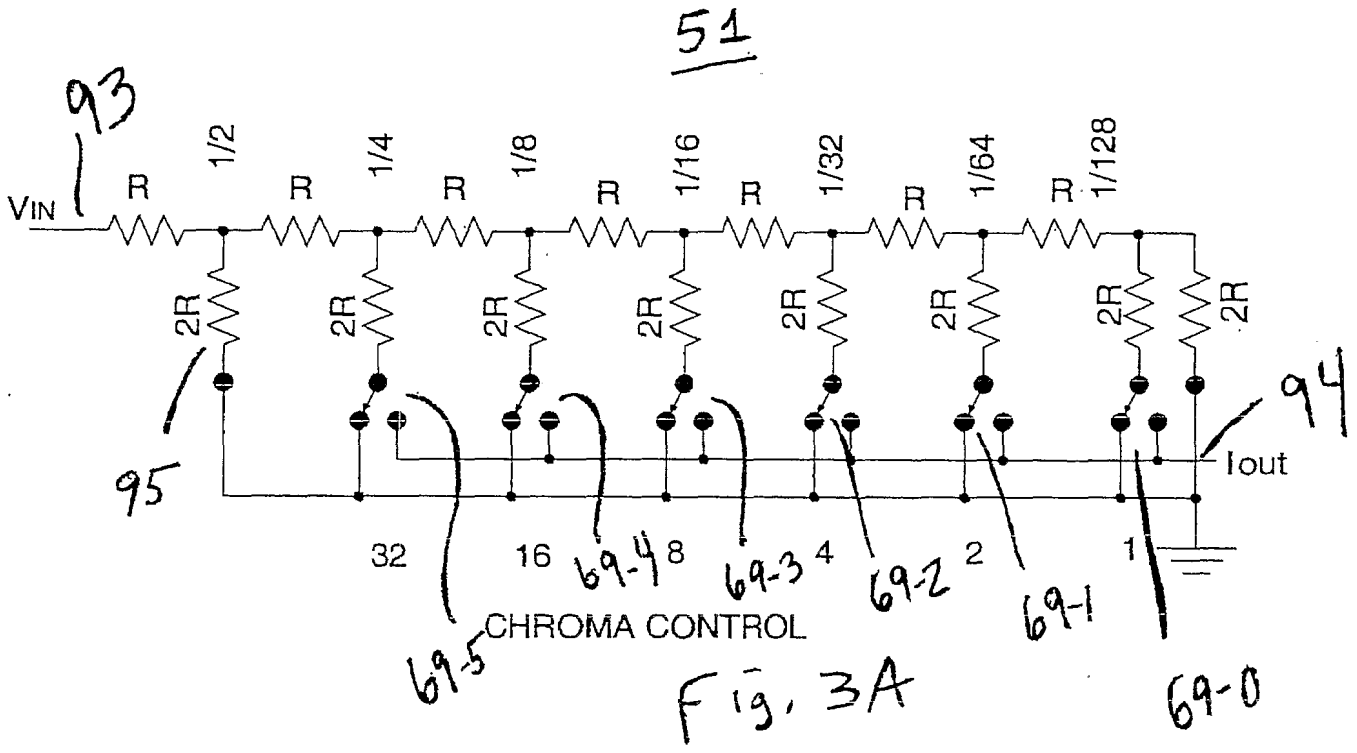

51
93
VIN
R
1/2
1/4
1/8
1/16
1/32
1/64
1/128
2R
95
94
Iout
32
16
8
4
2
1
69-4
69-3
69-2
69-1
69-0
69-5
CHROMA CONTROL

Fig. 3A

51

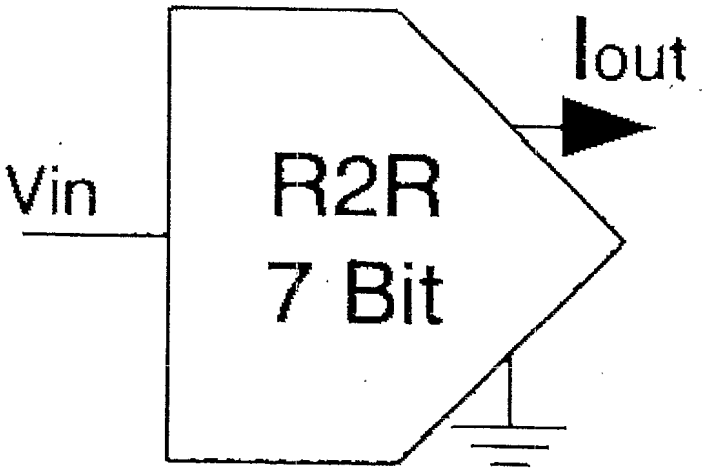


Fig. 3B

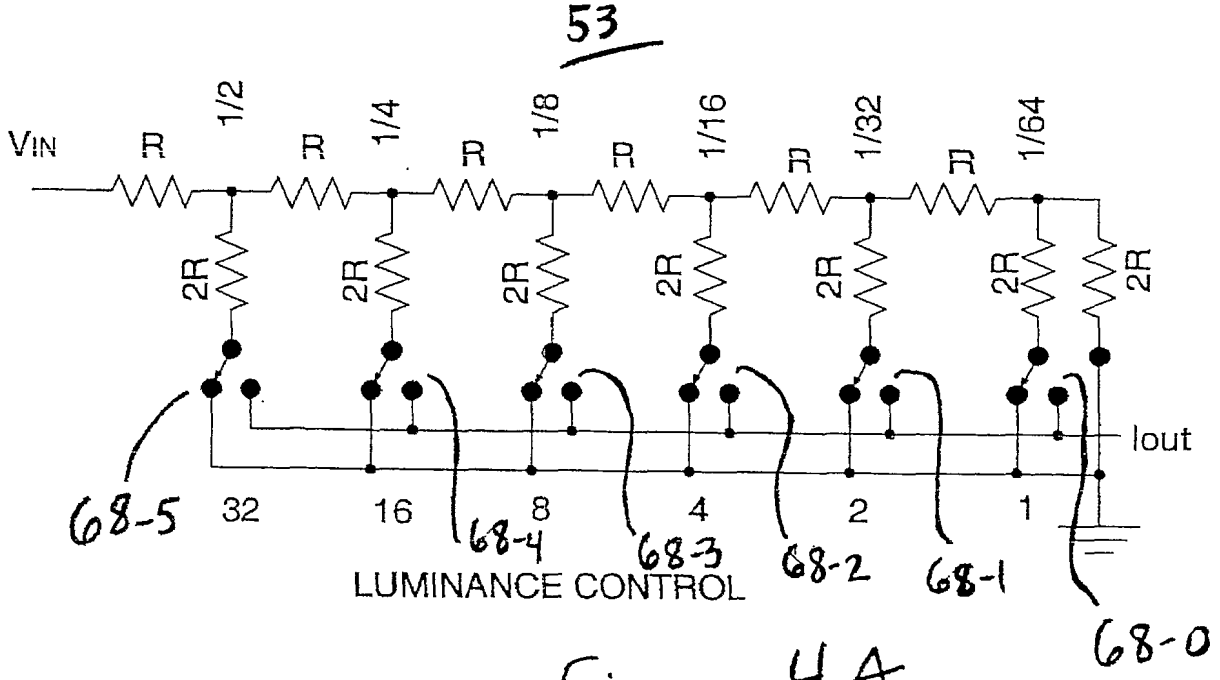

53
VIN
R
1/2
1/4
1/8
1/16
1/32
1/64
2R
Iout
68-5
32
16
8
4
2
1
68-4
68-3
68-2
68-1
68-0
LUMINANCE CONTROL

Fig. 4A

53

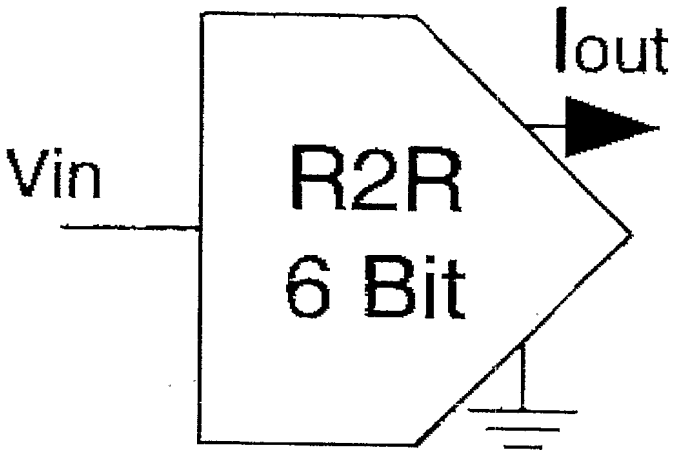


Fig. 4B

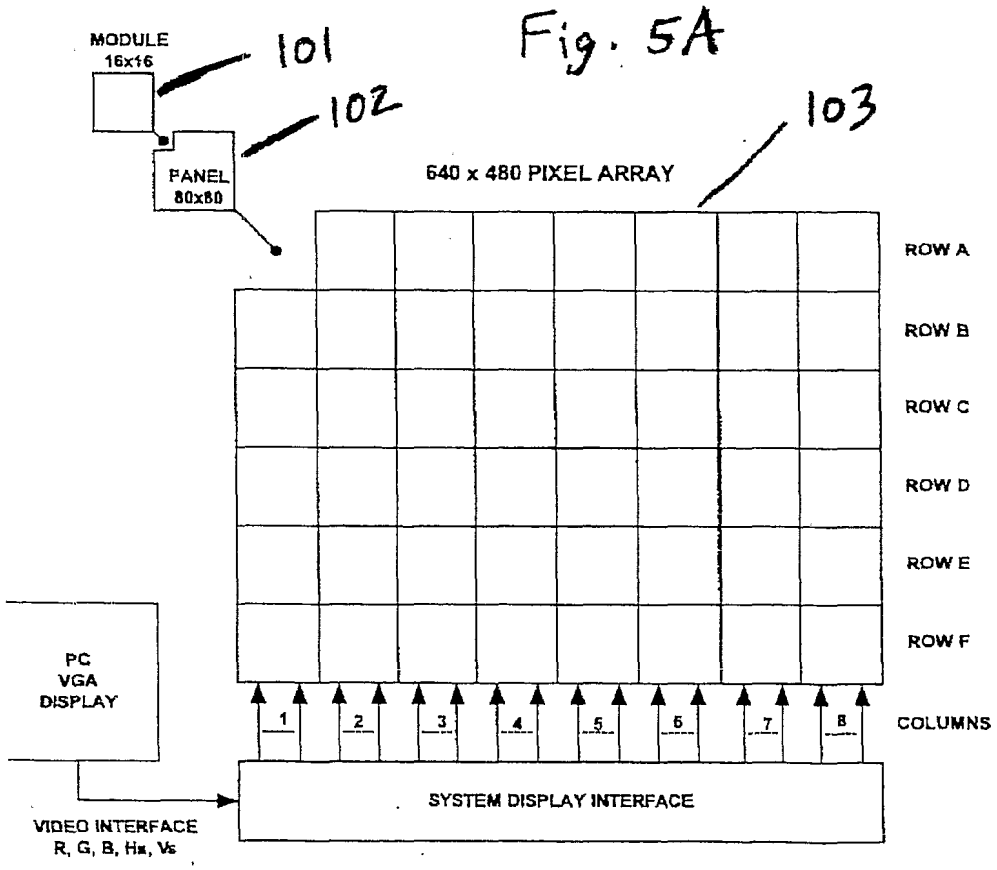

MODULE
16x16
101
102
PANEL
80x80
640 x 480 PIXEL ARRAY
103
ROW A
ROW B
ROW C
ROW D
ROW E
ROW F
COLUMNS
1
2
3
4
5
6
7
8
PC
VGA
DISPLAY
SYSTEM DISPLAY INTERFACE
VIDEO INTERFACE
R, G, B, Hs, Vs

Fig. 5A

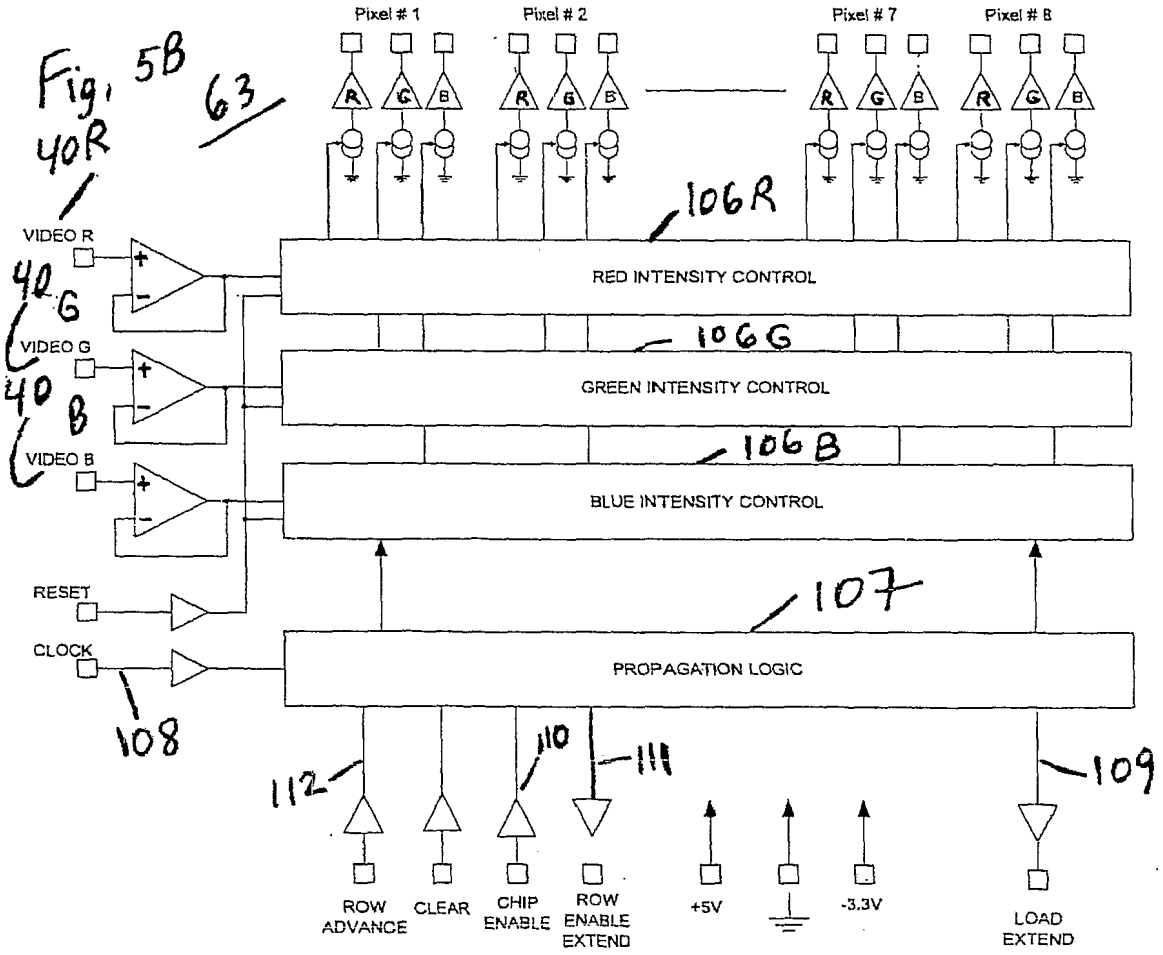


Fig. 5B

63

40R

40G

40B

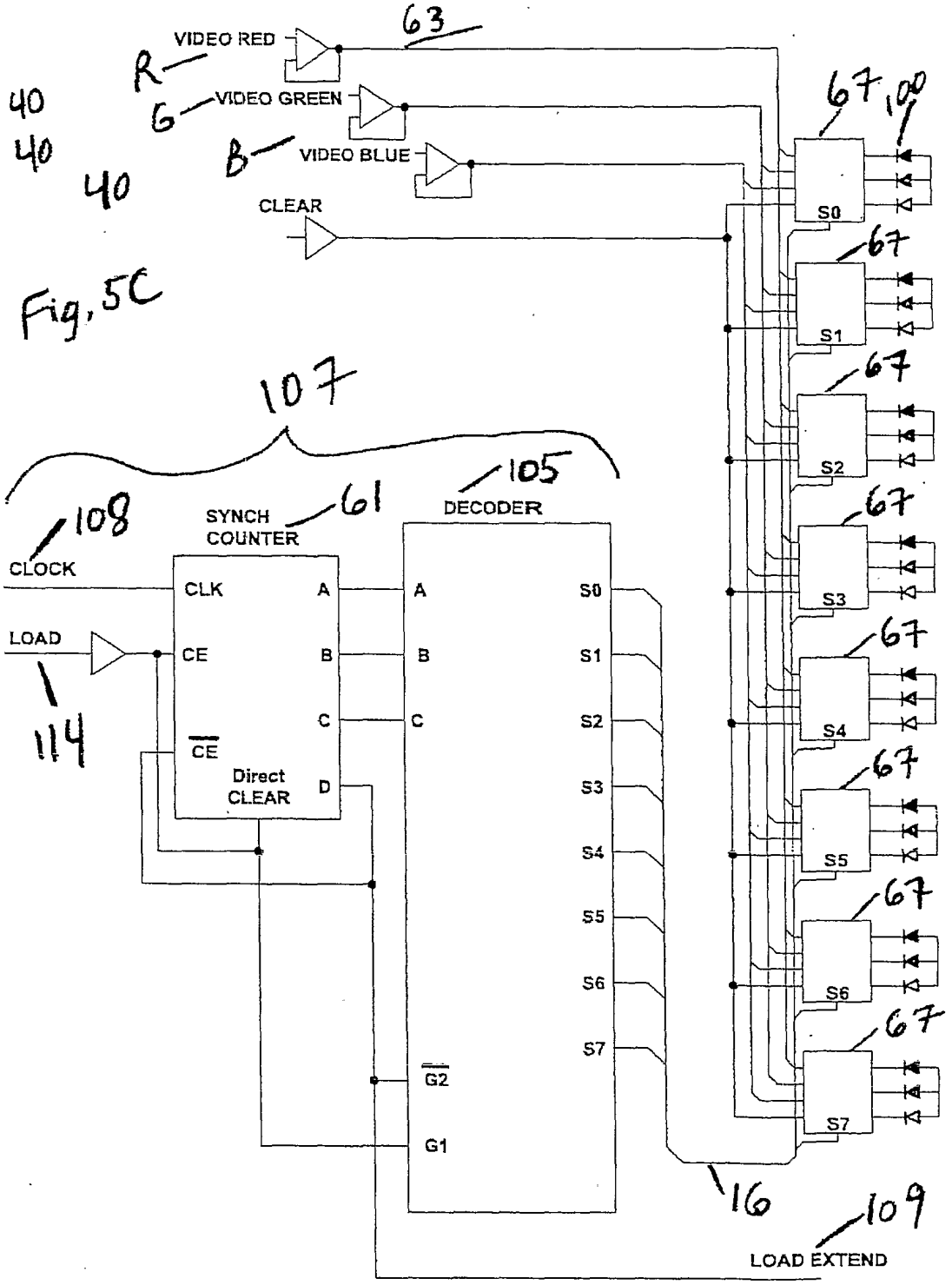
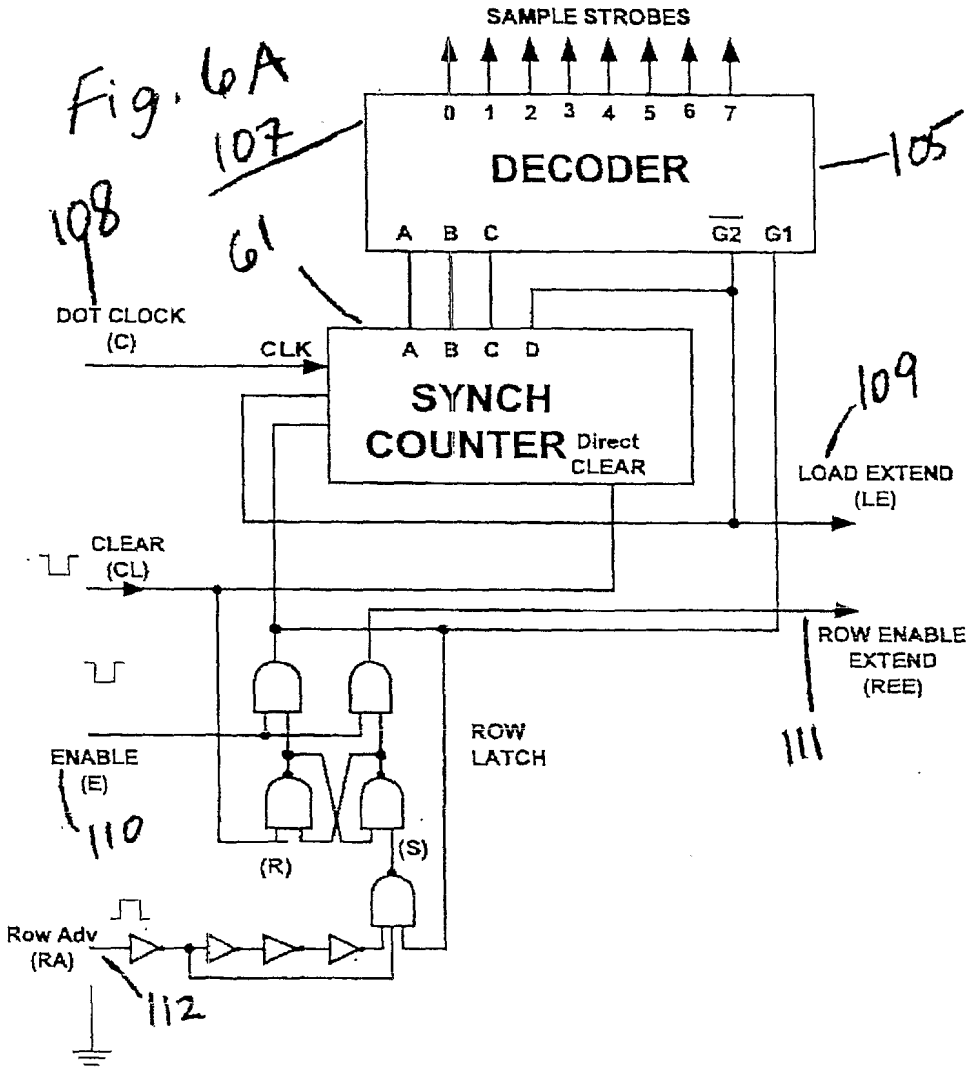

VIDEO RED
R
VIDEO GREEN
G
VIDEO BLUE
B
CLEAR
63
40
40
40
67
100
S0
S1
S2
S3
S4
S5
S6
S7
107
105
DECODER
108
CLOCK
SYNCH
COUNTER
61
CLK
CE
CE
Direct
CLEAR
A
B
C
D
LOAD
114
A
B
C
G2
G1
S0
S1
S2
S3
S4
S5
S6
S7
16
109
LOAD EXTEND

Fig. 5C

Fig. 6A


SAMPLE STROBES
0 1 2 3 4 5 6 7
DECODER
105
107
A B C
G2 G1
108
61
DOT CLOCK
(C)
CLK
A B C D
SYNCH
COUNTER
Direct
CLEAR
109
LOAD EXTEND
(LE)
CLEAR
(CL)
ROW ENABLE
EXTEND
(REE)
111
ROW
LATCH
ENABLE
(E)
110
(R)
(S)
Row Adv
(RA)
112

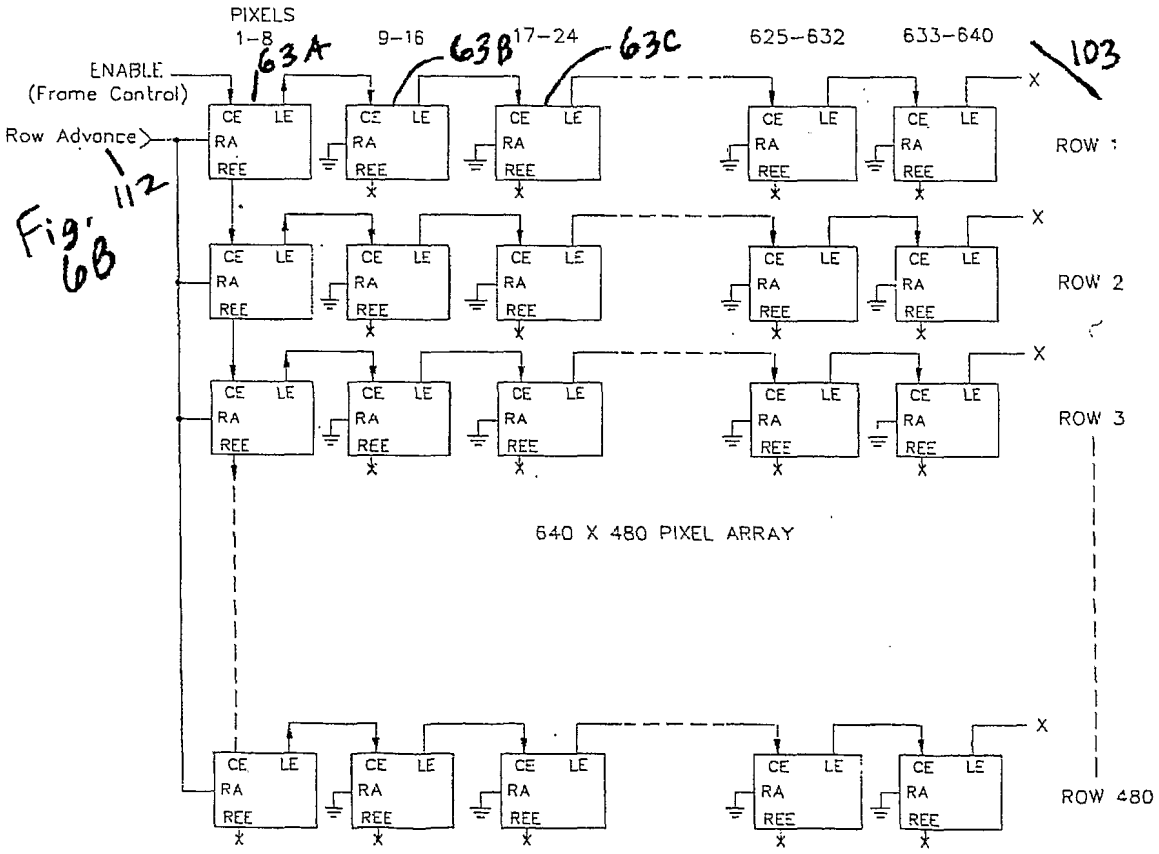

PIXELS
1-8
63A
9-16
63B
17-24
63C
625-632
633-640
103
ENABLE
(Frome Control)
Row Advance
112
CE
LE
RA
REE
X
ROW 1
ROW 2
ROW 3
ROW 480
640 X 480 PIXEL ARRAY

Fig. 6B

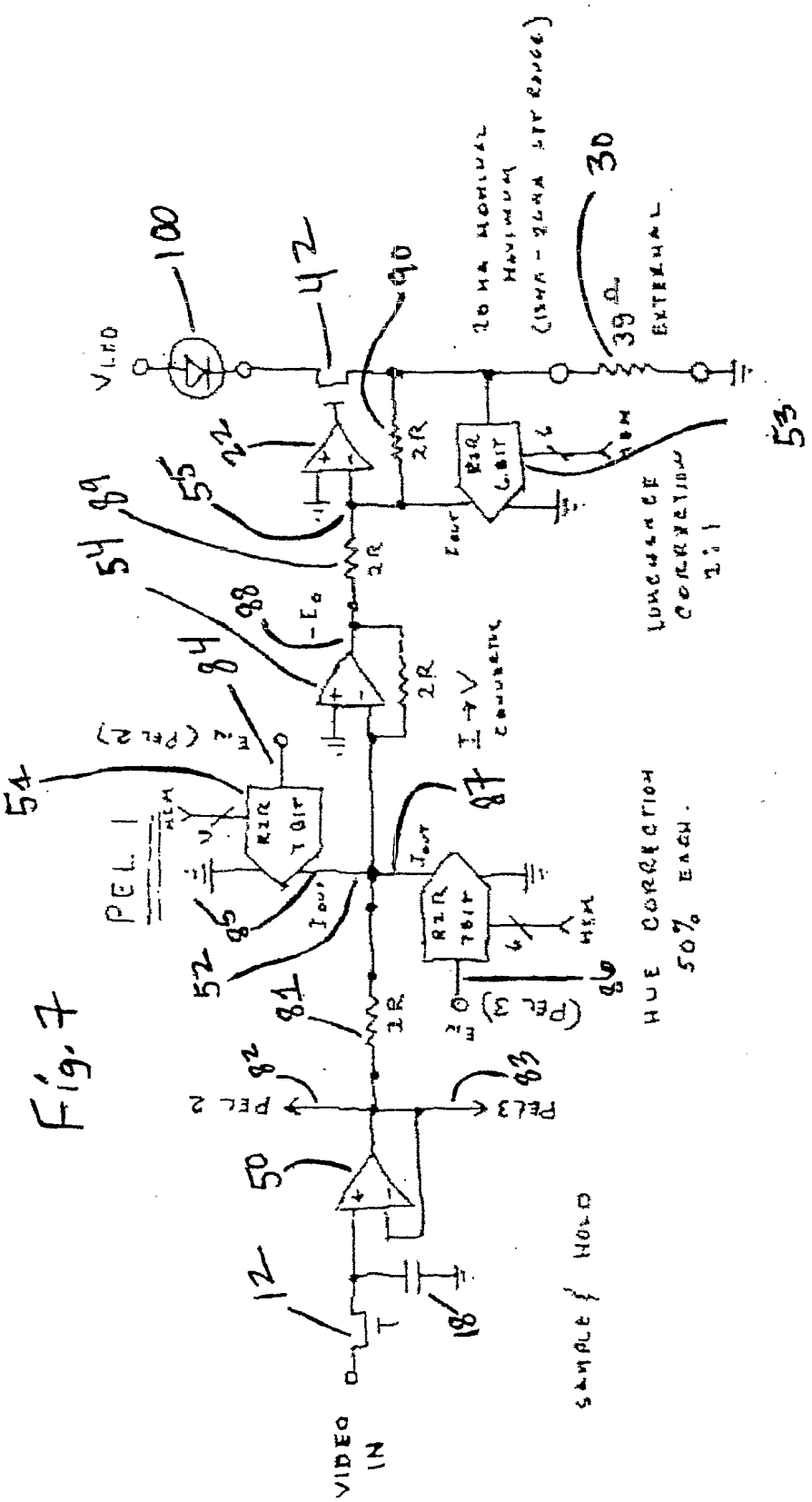
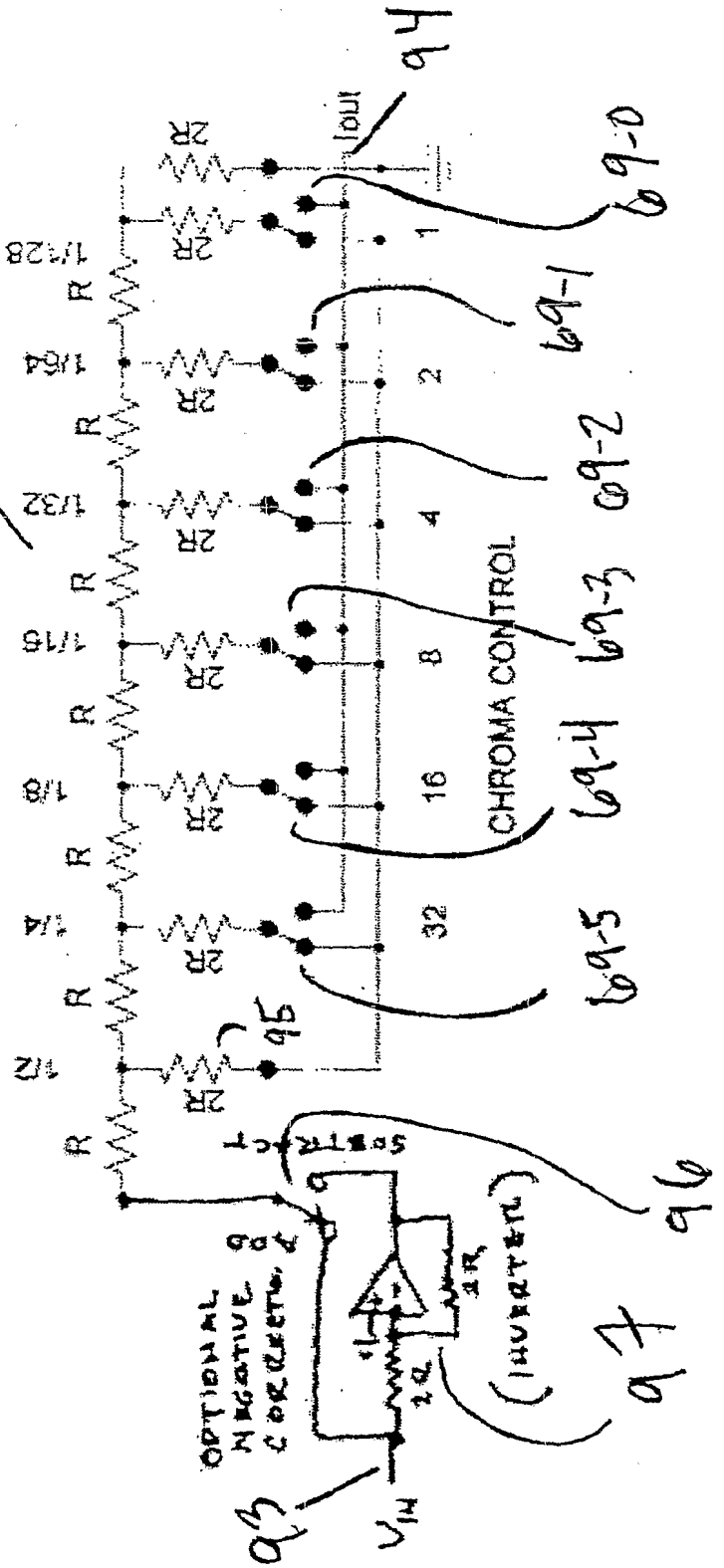

VLED
100
47
90
10 MA NOMINAL MAXIMUM (15MA - 2MA ADJ RANGE)
30
39Ω
EXTERNAL
53
22
55
99
54
2R
R2R 6 BIT
LUMINANCE CORRECTION 2:1
98
$-E_o$
84
I → V CONVERTER
E_2 (PEL 2)
54
87
PEL 1
R2R 7 BIT
HSM
I_{out}
85
52
81
2R
R2R 7 BIT
HSM
(PEL 3)
89
HUE CORRECTION 50% EACH.
82
PEL 2
PEL 3
83
50
SAMPLE & HOLD
12
18
VIDEO IN

Fig. 7

Fig. 8


92
94
69-0
69-1
69-2
69-3
69-4
69-5
CHROMA CONTROL
95
97
96
93
OPTIONAL NEGATIVE COEFFICIENT
(INVERTER)
2R
R
1/128
1/64
1/32
1/16
1/8
1/4
1/2
1
2
4
8
16
32

CORRECTION VALUES 07/22/2003

COL ①	x	y	OBJECTIVE - 6500 K 1%	Intensity cd/sq Mtr	TYPICAL x ⑥	y ⑦	6500K 1%	Intensity cd/sq Mtr ⑨	RED Correction ⑩	GREEN Correction ⑪	BLUE Correction ⑫
Red	0.670	0.330	[illegible]	[illegible]	0.700	0.300	[illegible]	546.2	0.857	0.030	0.065
Green	0.210	0.710	[illegible]	[illegible]	0.170	0.700	[illegible]	[illegible]	0.145	0.977	[illegible]
Blue	0.140	0.050	[illegible]	[illegible]	0.130	0.075	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
White				2000.0				2000.0			
Check Sum			1				1		1	1	1

RG, RB, GR, GB, BR, BG

Corrected Red	RED	[illegible]	RED display 1 times RED Correction factor for Red
	GREEN	[illegible]	RED display 1 times RED correction factor for Green
	BLUE	[illegible]	RED display 1 times RED correction factor for Blue
Corrected Green	RED	[illegible]	GREEN display 1 times Green Correction factor for Red
	GREEN	[illegible]	GREEN display 1 times Green correction factor for Green
	BLUE	[illegible]	GREEN display 1 times Green correction factor for Blue
Corrected Blue	RED	[illegible]	BLUE display 1 times BLUE Correction factor for Red
	GREEN	[illegible]	BLUE display 1 times BLUE correction factor for Green
	BLUE	[illegible]	BLUE display 1 times BLUE correction factor for Blue
NTSC WHITE	RED	[illegible]	ACUTAL RED equals sum of Corrected REDs
	GREEN	[illegible]	ACUTAL GREEN equals sum of Corrected GREENs
Sum Corrected Reds, Greens, and Blues	BLUE	[illegible]	ACUTAL BLUE equals sum of Corrected BLUEs
	Check Sum	1	

Fig. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US03/39647

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : G09G 3/30, 3/32, 5/00; H05B 37/00
US CL : 345/76,77,78,82,83,204,206,690; 315/312, 169.1, 169.2, 169.3

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 345/76,77,78,82,83,204,206,690; 315/312, 169.1, 169.2, 169.3

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EAST, WEST, JOP. Search terms: LED driver, brightness, luminance, correction, chrominance...

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	Pub. No.: US 2003/0016198 A1 (NAGAI et al.) 23 Jan 2003, [0082]-[0094], [0101]-[0103], [0143]-[0144], and [0151].	1-47

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search
19 August 2004 (19.08.2004)

Date of mailing of the international search report
10 SEP 2004

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Form PCT/ISA/210 (second sheet) (July 1998)