(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
20 November 2003 (20.11.2003)

PCT

(10) International Publication Number
WO 03/096353 A1

(51) International Patent Classification[7]: G11C 7/00, H01H 85/00, G01R 19/00, H01L 29/00

(21) International Application Number: PCT/US02/21267

(22) International Filing Date: 3 July 2002 (03.07.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/379,377 8 May 2002 (08.05.2002) US

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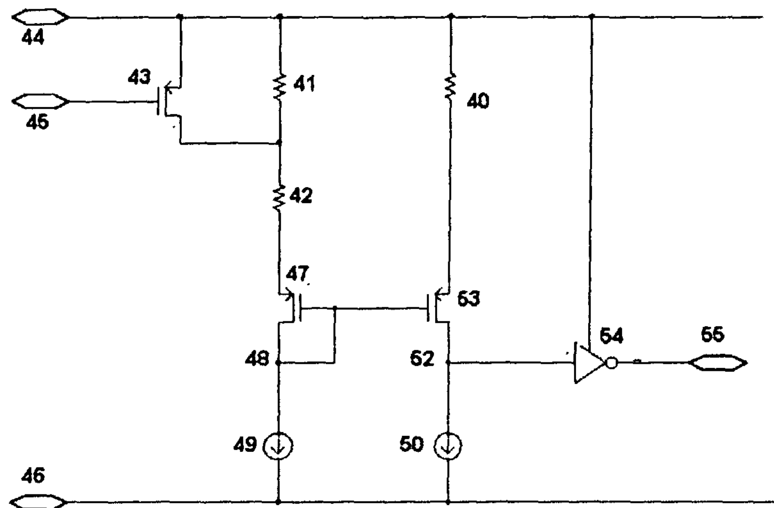
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) **Title:** METHOD AND APPARATUS FOR IMPROVING THE RELIABILITY OF THE READING OF INTEGRATED CIRCUIT FUSES



(57) **Abstract:** A system is provided for use with an on-chip fuse. If the fuse (40) is to be blown, the system blows the fuse, then performs a test read by comparing it with a larger-than-normal reference resistance (41, 42). If, even using the larger-than-normal reference resistance, the fuse reads as blown, then it is possible to be much more confident that the fuse will read correctly when compared against the normal reference resistance (42), even with aging and with variations of temperature and supply. For future reads during normal operation, the system compares it with the normal reference resistance (42). If, on the other hand, the fuse does not read as blown during the test read then the device can be rejected as a failed device.

WO 03/096353 A1

Method and apparatus for improving the reliability of the reading of integrated circuit fuses

This application claims priority from US appl. no. 60/379,377 entitled "Method for improving the reliability of integrated circuit fuse reading" and filed May 8, 2002, which
5 application is incorporated herein by reference.

Background

The application relates generally to blowing and reading fuses formed within integrated
10 circuits, and relates particularly to reading the fuses in a way that has improved reliability.

In many systems it is desirable to have a nonvolatile memory. In some applications a static RAM with a backup battery will be suitable, and in other applications an EEPROM may be suitable. But in recent times there has been great pressure on system designers to reduce the
15 size and power consumption of a system. Such pressure is particularly great with cellular telephones, personal digital assistants (PDAs), and notebook computers. In such a system, any decision that adds to the bulk or weight is undesirable, for example a decision to increase the chip count (to accommodate an external memory) or a decision to add a backup battery for a memory.

20

The general goal of reducing chip count provides motivation to try to use nonvolatile memory devices which can be fabricated within some existing chip in the system. One technology for such memory is the use of fuses. One or more fuses are fabricated within the chip. Circuitry is provided which will pass some specified current through the fuse, which "blows" the fuse.
25 Other circuitry measures the resistance of the fuse. If the resistance is low, then it is presumed that the fuse has not been blown. If the resistance is high, then it is understood that the fuse has been blown. Each fuse represents one binary data bit, and its blown or non-blown state is defined as a logic level of the binary data bit.

30 Several technologies for on-chip fuses have been proposed and used. One commonly used technology is a polysilicon fuse. A high current is passed through the fuse which "blows" the

fuse. As will be appreciated, it is necessary to distinguish later between the "blown" and "non-blown" conditions of the fuse.

It is desirable that the fuse, in its unblown state, have a low impedence, because this makes it
5 easier to get sufficiently high current through the fuse to blow it. It is also desirable that the fuse be constructed in a way that minimizing explosive decomposition which could result in damage to adjacent or nearby circuit structires.

Where a CMOS process is being used to fabricate the chip, to reduce the resistance of the
10 polysilicon fuse in its non-blown state, the fuse is manufactured with Ti-silicide doping. The Ti-silicide doping has the advantage not only of reducing the unblown impedence, but also of minimizing or eliminating explosive decomposition of the fuse.

While Ti-silicide doping has the advantage of reducing the unblown resistance and resisting
15 explosive decomposition, it has a potential drawback in that it "blowing" such a fuse results only in a process of silicide agglomeration once the fuse heats up to around 800°C. This results in the fuse undergoing a phase change of state which results in the fuse impedance changing from its unblown state of around 100 ohms to its blown state of any value from around 1KΩ to 500KΩ. This means that it is not easy to know exactly what resistance in the
20 fuse represents a "blown" state.

A typical way of reading the fuse (determining whether it is blown or unblown, that is, whether it represents a binary "1" or binary "0" value) is to compare the value of the fuse impedance with a fixed reference resistance. If the fuse impedance is greater than the
25 reference then it is read as blown, otherwise it is read as unblown. The comparison can be achieved by a number of techniques, but the most obvious is to force identical currents through the fuse and the reference resistor and to compare the resultant voltages using some form of voltage comparator.

30 Experience shows that such a blown fuse may change its resistance slightly with temperature or aging. This means that if a blown fuse impedance is very close to the reference resistance

then it may read as blown one time then as unblown another time. Such a result is extremely undesirable.

It will be appreciated that while this problem is described in particular connection with
5 polysilicon fuses, it presents itself with any fuse technology in which a blown fuse does not blow to a very high impedence.

It would be advantageous if an approach could be developed which permits determining, before a chip is placed into service, whether the chip is likely to provide a reliable reading of
10 its fuses. If such an approach were available, it could be used to test a chip; if the chip turned out to be unlikely to provide reliable reading of its fuses, a decision could be made not to place the chip into service.

Summary of the Invention

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A system is provided for use with an on-chip fuse. If the fuse is to be blown, the system blows the fuse, then performs a test read by comparing it with a larger-than-normal reference resistance. If, even using the larger-than-normal reference resistance, the fuse reads as blown, then it is possible to be much more confident that the fuse will read correctly when compared
20 against the normal reference resistance, even with aging and with variations of temperature and supply voltage. For future reads during normal operation, the system compares it with the normal reference resistance. If, on the other hand, the fuse does not read as blown during the test read then the device can be rejected as a failed device.

25
Description of the drawing

Fig. 1 is a schematic diagram of an embodiment of the invention.

Detailed description

30

Fig. 1 is a schematic diagram of an embodiment of the invention, with some detail omitted for clarity.

Fuse 40 is, in an exemplary embodiment, a polysilicon fuse. To read the fuse 40, the system
5 compares the resistance of the fuse 40 with a reference resistance. The reference resistance is set by resistors 42 and 41, which may be 1KΩ and 500Ω respectively. During the test read, PMOS transistor switch 43 is turned off and the reference resistance becomes 1KΩ plus 500Ω giving a total resistance of 1.5KΩ. During normal reads, transistor 43 is turned on which shorts out resistor 41, and therefore the reference resistance is only 1 K ohms plus a small
10 switch resistance. The embodiment assumes a positive voltage V_{DD} 44 and a ground 46.

PMOS transistor 43 is controlled by a "test read" signal 45.

Reading is achieved by enabling the current sinks 49 and 50. These sink identical currents
15 (I_{REF}) through the fuse 40 and the reference resistance via gain transistors 53 and 47 respectively.

If the impedance of the fuse 40 is lower than the reference resistance (that is, if we are assuming it to be an unblown fuse) then transistor 53 is turned on more than transistor 47
20 which causes node 52 to rise which results in the data output 55 reading a logic 0.

If the impedance of the fuse 40 is higher than the reference resistance (that is, if are assuming it to be a blown fuse) then transistor 53 is turned on less than transistor 47 which causes node 52 to fall which results in the data output 55 reading a logic 1.

25

Omitted for clarity in Fig. 1 is an additional gain stage between node 52 and gate 54 to enhance sensitivity of the system.

Another configuration for implementing the comparison is to have the fuse 40 and reference
30 resistor 41, 42 connected to ground 46. The gain transistors are NMOS instead of PMOS in this configuration, and the current references are connected to the supply voltage 44.

Yet another configuration is to force the reference currents directly across the fuse 40 and reference resistor 41, 42 rather than through gain transistors 47, 53. In this configuration, the resultant voltages at nodes 48, 52 are fed into a standard voltage comparator.

5 In a typical application of the invention, the test read is used before the chip is placed into service. That is, the test read will only be done during production testing and so this function can be transparent to the end user, that is, un-noticed by the end user.

The net benefit to the user is that the observed reliability of fuse reading is greatly enhanced.

10

It should be appreciated that the invention offers its benefits in situations where there is more than one fuse. Indeed in many chips it is expected that there will be several such fuses. Thus a typical sequence of steps may be performed, for example, with respect to a first fuse and a second fuse within an integrated circuit. Current is passed through the first fuse, thereby 15 blowing the first fuse. Current is passed through the second fuse, thereby blowing the second fuse. The resistance of the first fuse is compared with a higher resistance than the reference resistance. The resistance of the second fuse is compared with the higher resistance. In the event that the resistance of the first fuse turns out to be higher than the higher resistance and the resistance of the second fuse turns out to be higher than the higher resistance, the 20 integrated circuit is placed into service.

Later, after the integrated circuit is placed into service, from time to time the resistance of the first fuse is compared with the reference resistance, and the resistance of the second fuse is compared with the reference resistance.

25

It should be appreciated that another possible outcome of the test read is that the resistance of the first fuse will turn out to be lower than the higher resistance, or the resistance of the second fuse will turn out to be lower than the higher resistance. In that event, a decision is made that the integrated circuit will not be placed into service.

30

An exemplary apparatus will now be described with reference to Fig. 1. The apparatus

comprises a fuse 40 having a resistance, a first reference resistance 42, and a second reference resistance 41, 42 greater than the first reference resistance 42.

In a first embodiment, a first constant-current reference 49 is connected in series with first
5 and second resistors 42, 41 with a first MOSFET transistor 47 with source and drain between the first constant-current reference 49 and the first and second resistors 42, 41, a connection between the first constant-current reference 49 and the first MOSFET transistor 47 defining a first node 48. In addition, a second constant-current reference 50 is connected in series with the fuse 40 with a second MOSFET transistor 53 with source and drain between the second
10 constant-current reference 50 and the fuse 40, a connection between the second constant-current reference 50 and the second MOSFET transistor 53 defining a second node 52. A switch 43 is in parallel with the second resistor 41. The gates of the first and second MOSFET transistors 47, 53 are connected together and to the first node 48. In this embodiment the first resistor 42 defines the first reference resistance, and the series-wise
15 combination of the first and second resistors 42, 41 defines the second (higher) reference resistance. The second node 52 defines an output of the apparatus, and may be provided to an inverter 54 having a logic output 55. Positive supply voltage 44 and negative supply voltage 46 are provided. As may be seen in Fig. 1, the series-wise combination of the first and second resistors 42, 41 is connected to the positive supply voltage 44. The fuse 40 is also
20 connected to the positive supply voltage 44. The first constant-current reference 49 is a current sink and is also connected to the negative supply voltage 46. The second constant-current reference 50 is a current sink and is also connected to the negative supply voltage 46. In this embodiment, the MOSFET transistors 47, 53 are PMOS.

25 In a second embodiment, the series-wise combination of the first and second resistors is connected to the negative supply voltage, and the is fuse also connected to the negative supply voltage. The first constant-current reference is a current source also connected to the positive supply voltage. The second constant-current reference is a current source also connected to the positive supply voltage. The MOSFET transistors are NMOS.

30

In a third embodiment, a first constant-current reference is connected in series with the first

and second resistors, and a connection between the first constant-current reference and the first and second resistors defines a first node. A second constant-current reference is connected in series with the fuse, and a connection between the second constant-current reference and the fuse defines a second node. The first resistor defines the first reference resistance, and the series-wise combination of the first and second resistors defining the second reference resistance. A comparator receiving as inputs signals from the first and second nodes, and its output defines an output of the apparatus.

It should be appreciated that those skilled in the art will have little difficulty devising obvious variations of the invention, all of which are to be encompassed by the claims that follow.

Claims

What is claimed is:

5 1. A method for blowing and testing a first fuse and a second fuse within an integrated circuit, the resistance of the first fuse to be compared with a reference resistance when the integrated circuit is in service, the resistance of the second fuse to be compared with the reference resistance when the integrated circuit is in service, the method comprising the steps of:

10

passing current through the first fuse, thereby blowing the first fuse;

passing current through the second fuse, thereby blowing the second fuse;

15 comparing the resistance of the first fuse with a higher resistance than the reference resistance;

comparing the resistance of the second fuse with the higher resistance;

20 in the event of the resistance of the first fuse being higher than the higher resistance and the resistance of the second fuse being higher than the higher resistance, placing the integrated circuit into service.

2. The method of claim 1 further comprising the step of:

25

comparing the resistance of the first fuse with the reference resistance.

3. The method of claim 2 further comprising the step of:

30 comparing the resistance of the second fuse with the reference resistance.

4. A method for blowing and testing a first fuse and a second fuse within an integrated circuit, the resistance of the first fuse to be compared with a reference resistance when the integrated circuit is in service, the resistance of the second fuse to be compared with the reference resistance when the integrated circuit is in service, the method comprising the steps
5 of:

passing current through the first fuse, thereby blowing the first fuse;

passing current through the second fuse, thereby blowing the second fuse;
10

comparing the resistance of the first fuse with a higher resistance than the reference resistance;

comparing the resistance of the second fuse with the higher resistance;
15

in the event of the resistance of the first fuse being lower than the higher resistance or the resistance of the second fuse being lower than the higher resistance, not placing the integrated circuit into service.

20 5. A method for blowing and testing a fuse within an integrated circuit, the resistance of the fuse to be compared with a reference resistance when the integrated circuit is in service, the method comprising the steps of:

passing current through the fuse, thereby blowing the fuse;
25

comparing the resistance of the fuse with a higher resistance than the reference resistance;

in the event of the resistance of the fuse being higher than the higher resistance, placing the integrated circuit into service.

30

6. The method of claim 5 further comprising the step of:

comparing the resistance of the fuse with the reference resistance.

7. A method for blowing and testing a fuse within an integrated circuit, the resistance of the fuse to be compared with a reference resistance when the integrated circuit is in service, the
5 method comprising the steps of:

passing current through the fuse, thereby blowing the fuse;

comparing the resistance of the fuse with a higher resistance than the reference resistance;
10

in the event of the resistance of the fuse being lower than the higher resistance, not placing the integrated circuit into service.

8. Apparatus formed on an integrated circuit comprising:
15

a fuse having a resistance;

a first reference resistance;

20 a second reference resistance greater than the first reference resistance;

first means responsive to a comparison of the first reference resistance with the fuse for providing an output indicative of whether the resistance of the fuse is greater than the first reference resistance; and
25

second means responsive to a comparison of the second reference resistance with the fuse for providing an output indicative of whether the resistance of the fuse is greater than the first reference resistance.

30 9. The apparatus of claim 8 wherein the first and second means comprise:

a first constant-current reference connected in series with first and second resistors with a first MOSFET transistor with source and drain between the first constant-current reference and the first and second resistors, a connection between the first constant-current reference and the first MOSFET transistor defining a first node;

5

a second constant-current reference connected in series with the fuse with a second MOSFET transistor with source and drain between the second constant-current reference and the fuse, a connection between the second constant-current reference and the second MOSFET transistor defining a second node;

10

a switch in parallel with the second resistor;

gates of the first and second MOSFET transistors connected together and to the first node;

15 the first resistor defining the first reference resistance, and the series-wise combination of the first and second resistors defining the second reference resistance;

the second node defining an output of the apparatus.

20 10. The apparatus of claim 9 further comprising positive and negative supply voltages,

the series-wise combination of the first and second resistors also connected to the positive supply voltage;

25 the fuse also connected to the positive supply voltage;

the first constant-current reference comprising a current sink also connected to the negative supply voltage;

30 the second constant-current reference comprising a current sink also connected to the negative supply voltage;

the MOSFET transistors characterized as PMOS.

11. The apparatus of claim 9 further comprising positive and negative supply voltages,

5 the series-wise combination of the first and second resistors also connected to the negative supply voltage;

the fuse also connected to the negative supply voltage;

10 the first constant-current reference comprising a current source also connected to the positive supply voltage;

the second constant-current reference comprising a current source also connected to the positive supply voltage;

15

the MOSFET transistors characterized as NMOS.

12. The apparatus of claim 8 wherein the first and second means comprise:

20 a first constant-current reference connected in series with first and second resistors, a connection between the first constant-current reference and the first and second resistors defining a first node;

a second constant-current reference connected in series with the fuse, a connection between 25 the second constant-current reference and the fuse defining a second node;

a switch in parallel with the second resistor;

the first resistor defining the first reference resistance, and the series-wise combination of the 30 first and second resistors defining the second reference resistance;

a comparator receiving as inputs signals from the first and second nodes,

an output of the comparator defining an output of the apparatus.

5 13. The apparatus of claim 8 wherein the fuse is a polysilicon fuse.

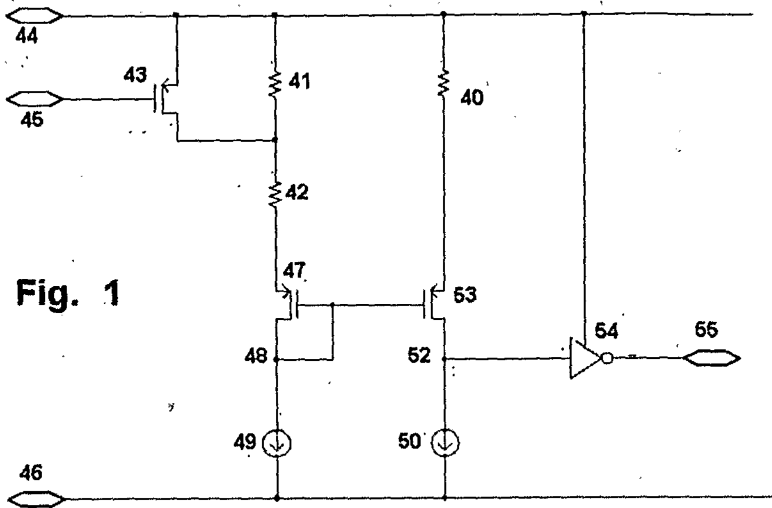
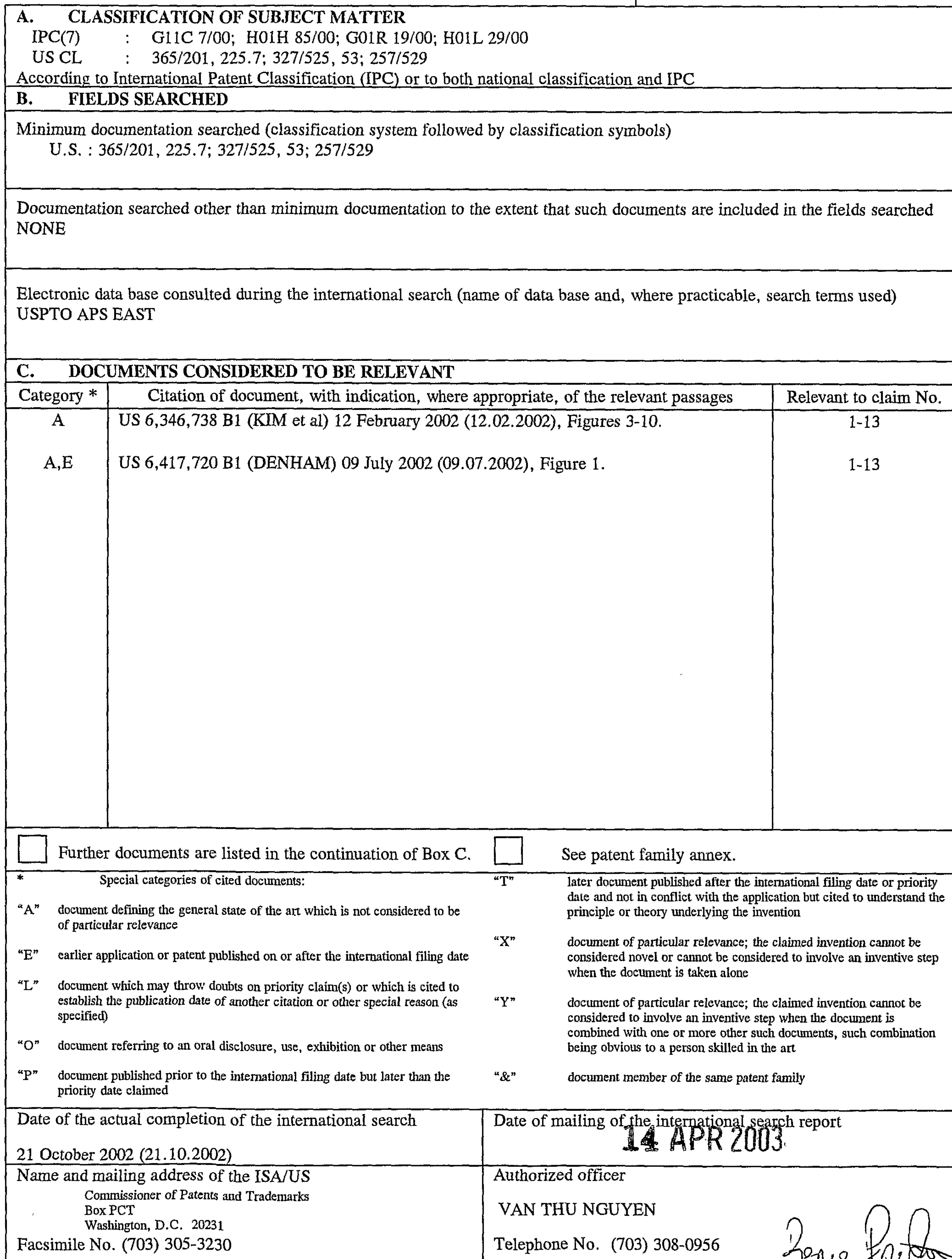


Fig. 1



INTERNATIONAL SEARCH REPORT

International application No.

PCT/US02/21267

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : G11C 7/00; H01H 85/00; G01R 19/00; H01L 29/00

US CL : 365/201, 225.7; 327/525, 53; 257/529

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 365/201, 225.7; 327/525, 53; 257/529

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6,346,738 B1 (KIM et al) 12 February 2002 (12.02.2002), Figures 3-10.	1-13
A,E	US 6,417,720 B1 (DENHAM) 09 July 2002 (09.07.2002), Figure 1.	1-13

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
21 October 2002 (21.10.2002)	14 APR 2003

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